Bipolar Ripple Cancellation Method to Achieve Single-Stage Electrolytic-Capacitor-Less High-Power LED Driver

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***Abstract*— Conventional topologies for high-power LED drivers with high power factors (PFs) require large capacitances to limit the low frequency (100 or 120 Hz) LED current ripples. Electrolytic capacitors are commonly used because they are the only capacitors with sufficient energy density to accommodate high-power applications. However, the short life span of electrolytic capacitors significantly reduces the life span of the entire LED lighting fixture, which is undesirable. This paper proposes a bipolar (ac) ripple cancellation method with two different full-bridge power structures to cancel the low-frequency ac ripple in the LED current and minimize the output capacitance requirement, enabling the use of long-life film capacitors. Compared with the existing technologies, the proposed circuit achieves zero double-line-frequency current ripple through LED lamps and achieves a high PF and high efficiency. A 100-W (150 V/0.7 A) LED driver prototype was built which demonstrates that the proposed method can achieve the same double-line-frequency LED current ripple with only 44-μF film capacitors, compared with the 4700-μF electrolytic capacitors required in the conventional single-stage LED drivers. Meanwhile, the proposed prototype has achieved a peak power efficiency of 92.5%, benefiting from active clamp technology.**

***Index Terms*— AC supplied LED drivers, full-bridge inverter, high-power LED drivers, single-stage power factor correction (PFC), zero 120-Hz ripple current.**

I. Introduction

With the LED lamp technology becoming mature, cost-effective, and energy-efficient power LED light will become dominant in the high-power lighting applications due to its high luminous flux, high efficacy, and long life span. The recent studies on the power supplies of LED bulb (LED drivers) are diverse including paralleled LED strings load sharing [1], [2], LED dimming [3], [4], and LED current ripple suppressing [4]. As an important branch of LED drivers study, ac-connected high-power LED drivers (V_{in} = 85–265 V_{ac}, P_O > 50 W) are commonly used in outdoor lighting applications, such as street lights, parking lot lights, and high-bay industrial lights. In these applications, a large number of LEDs are connected in series to increase the lumens. This configuration yields a high output voltage and low output current combination requirement for the drivers, and usually requires isolation.

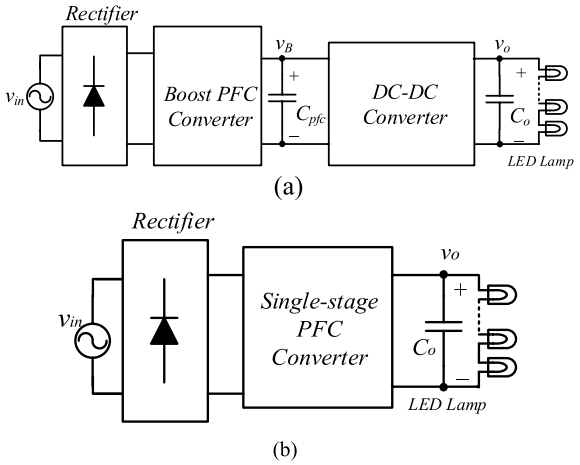

Fig. 1. Conventional high-power LED driver configurations. (a) Two-stage configuration. (b) Single-stage configuration.

The conventional LED driver solutions for high-power LED drivers include two categories: 1) two-stage configuration [5]–[7] and 2) single-stage configuration [8]–[10], as shown in Fig. 1.

The two-stage configuration, as shown in Fig. 1(a), can achieve high power factor (PF) and tight output current regulation, making it a mainstream solution for high-power LED drivers [11]. However, it exhibits a poor efficiency and low power density. Usually, capacitors of high capacitance value are needed at the output of the PF correction (PFC) stage to buffer the power difference of the ac input and dc output. The necessary capacitance is generally $\sim$1 μF/W [12]. The PFC output capacitance can be reduced by increasing the voltage ripple [12]. However, the possible capacitance reduction is limited because the PFC output voltage must be higher than the minimum input line voltage to ensure the normal operation of the boost PFC converter. Therefore, electrolytic capacitors are still required for high-power applications.

The conventional single-stage configuration, as shown in Fig. 1(b), presents a cost-effective and high-efficiency

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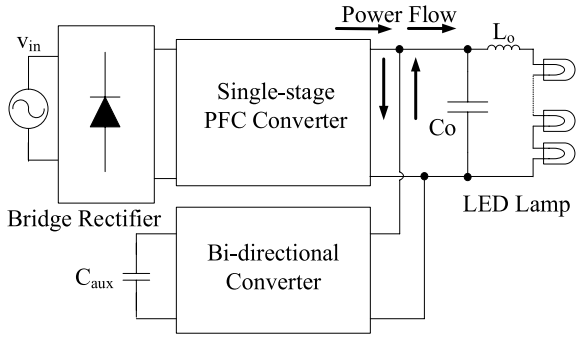


Fig. 2. Parallel ripple cancellation configuration.

solution, yet the large electrolytic capacitors are still necessary to reduce the double line frequency (100 or 120 Hz) current ripple. Otherwise, the double line frequency current ripple will cause light flickering, which is harmful to human visual system [13]–[15]. However, electrolytic capacitor is not desired in LED driver as it suffers from the deadly drawback of relatively short operating life (5000 h [16]), compared with the lifetime of LED lamp (>50 000 h [17]). According to [16], the electrolytic capacitor life is a function of operating temperature. As a rule of thumb, its life halves for each 10 °C higher operating temperature. Therefore, the unmatched-life-span problem becomes more serious for the outdoor power supply such as street light working in the extremely harsh environment. Some solutions have been proposed to reduce this ripple and remove the electrolytic capacitors.

One method is to inject the harmonics (third and fifth) into the input current [18], [19]. This sacrifices the PF, which is unacceptable for high-power LED drivers. In [20]–[23], an auxiliary ripple cancellation stage is connected in parallel with the PFC output to reduce the PFC output capacitance, as shown in Fig. 2. It is noted that the auxiliary stage must withstand the same high-voltage stress equal to the PFC output voltage. The voltage across the auxiliary capacitor (V_{aux}) is even higher. Therefore, high voltage-rating components are necessary, which generally have higher cost and lower efficiency than their low-voltage-rating counterparts. In addition, an output filter inductor L_O is required to be connected in series with the LED load to limit the LED current ripple.

In [24]–[26], the auxiliary stage is in series with the PFC output, thus the voltage stress can be reduced to the peak-to-peak (pk-to-pk) voltage ripple value. However, the room for capacitance reduction is also limited, since the ripple cancellation circuit is unipolar. The auxiliary stage must provide a large dc component to cancel a large PFC output voltage ripple. This increases the stress on the auxiliary circuit, which is also unfavorable to achieve high efficiency.

In this paper, a novel high-power single-stage LED driver configuration with a bipolar ripple cancellation stage is proposed. The bipolar ripple cancellation circuit is a full-bridge converter used to generate a pure ac voltage with zero dc bias which cancels the low-frequency voltage ripple of the PFC output. With this cancellation stage, the PFC output capacitance can be significantly reduced, allowing long-life power film capacitors [27] to be used. Two power structures are proposed to achieve the ripple cancellation. One is with an auxiliary transformer winding from the main power converter and the other is using a floating capacitor, without an auxiliary winding.

This paper is organized as follows. Section II introduces the proposed bipolar ripple cancellation principle and the basic control strategy for high-power LED driver configuration. Section III proposes the improved power architecture with floating capacitor to achieve the bipolar ripple cancellation without using the extra auxiliary winding from the main stage. Section IV provides the step-by-step design procedure. Section V describes the operation modes and advantages of the proposed bipolar ripple cancellation stage. Section VI provides the experimental results. Finally, the conclusion is drawn in Section VII.

II. Operation Principles of the Proposed Bipolar Ripple Cancellation Method

A. Basic Bipolar Ripple Cancellation Concept of Proposed LED Driver

Fig. 3 shows circuit block diagram of the proposed electrolytic-capacitor-less configuration for high-power LED driver. This configuration consists of a bridge rectifier, a single-stage PFC stage (main stage), and a bipolar ripple cancellation stage [full-bridge ripple cancellation converter (FB RCC)]. The main output voltage and the FB RCC output voltage are connected in series and the combined voltage is used to power the LED lamps. Fig. 3 also shows the voltage waveforms of the main output (v_{main}), ripple cancellation stage output (v_{FB}), and the LED voltage (V_{LED}).

The PFC output voltage, V_{main}, includes both the ac and dc voltage components. The ac voltage ripple is at double line frequency, shown as in Fig. 3 (red curve). The expression of the PFC output voltage is in

$$v_{\text{main}} = V_{\text{dc}} + v_{\text{ripple}} \tag{1}$$

where V_{dc} is the dc component of the PFC output voltage and v_{ripple} is the ac component of PFC output voltage. The output voltage of the cancellation stage v_{FB} is a pure ac voltage, shown in Fig. 3 (blue curve) with zero dc voltage. In order to achieve a ripple-free output voltage across the LED lamps, the cancellation voltage v_{FB}, must offset the voltage ripple, v_{ripple}, as given in

$$v_{\text{FB}}(t) = -v_{\text{ripple}}(t). \tag{2}$$

The voltage across the LED lamp is the sum of the PFC output voltage and the cancellation stage output voltage, expressed in

$$V_{\text{LED}} = v_{\text{main}} + v_{\text{FB}}. \tag{3}$$

Substitution of (1) and (2) into (3) yields

$$V_{\text{LED}} = V_{\text{dc}}. \tag{4}$$

The LED lamp sees only the dc component, as shown in Fig. 3 (brown line). It is noted that the pk-to-pk value of the

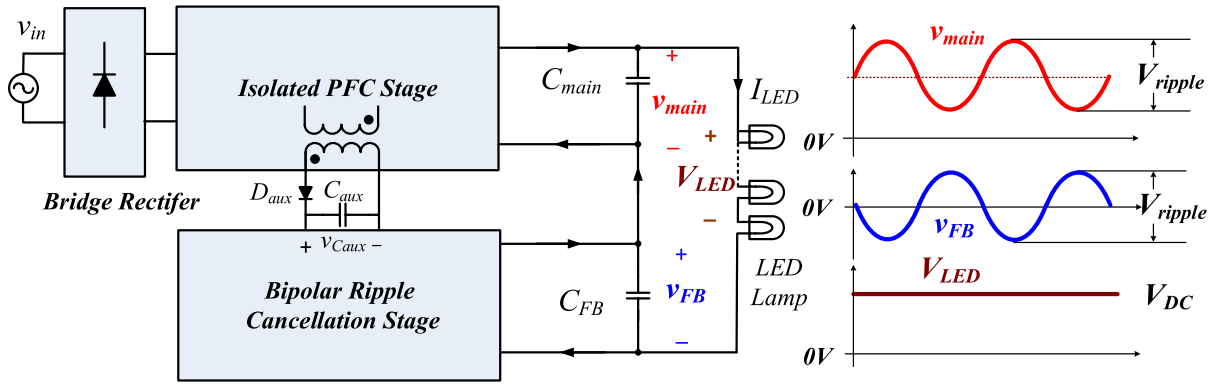


Fig. 3. Circuit block diagram of the proposed electrolytic-capacitor-less LED driver and the key waveforms of bipolar ripple cancellation.

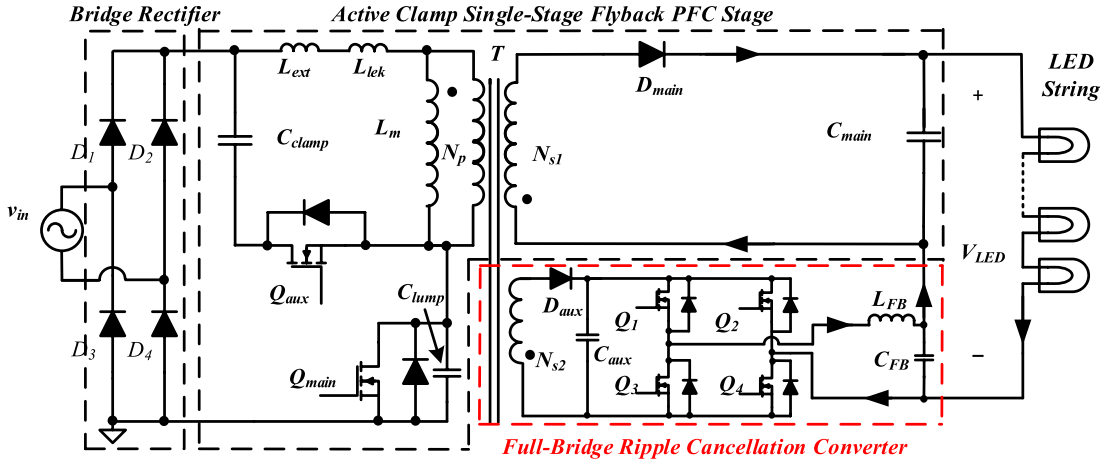


Fig. 4. Proposed electrolytic-capacitor-less LED driver architecture with FB RCC.

double line frequency voltage ripple in PFC output V_{ripple} is proportional to the LED output current I_{LED} as well as the PFC output capacitance C_{main}, as shown in

$$V_{\text{ripple}} = \frac{P_{\text{in}}}{\omega \times C_{\text{main}} \times V_{\text{LED}}} = \frac{I_{\text{LED}}}{2\pi \times f \times C_{\text{main}}}. \quad (5)$$

A smaller value of C_{main} should be used in order to remove the electrolytic capacitor from the proposed configuration, which will be discussed in Section IV.

A corresponding circuit diagram of the proposed LED driver is shown in Fig. 4, where a single-stage flyback circuit is selected as the isolated PFC stage in the prototype, while the auxiliary bipolar ripple cancellation stage is an FB RCC composed of four switches (Q_1–Q_4), one inductor (L_{FB}) and two capacitors (input capacitor C_{aux} and output capacitor C_{FB}). The flyback PFC provides all of the LED driving power as well as a small amount of power to the full-bridge converter. Therefore, active clamp technology [28]–[32] is used in this flyback circuit to enhance the overall system efficiency. The FB RCC only compensates the ac voltage ripple.

B. Control Strategy for Full-Bridge Ripple Cancellation Converter

As shown in Fig. 4, the input capacitor of the FB RCC (C_{aux}) is connected to the flyback PFC stage via a secondary transformer winding (N_{s2}) and a diode (D_{aux}). Fig. 5 shows the detailed control strategy to achieve the bipolar ripple cancellation.

The ripple component ($v_{\text{main\_ripple}}$) in the main output voltage (v_{main}) is sensed and scaled as the reference for the FB RCC after blocking the dc component using an analog differential circuit consists of a dc blocking capacitor and resistor, as shown in dc blocking unit in Fig. 5. With the PI control, the FB RCC is able to track the ac reference ($v_{\text{main\_ripple}}$) and rebuild a reversed ac output voltage (v_{FB}), which can fully cancel the double line frequency ripple in the main output voltage, as shown in Fig. 3.

C. LED Current Regulation and Power Factor Correction

The LED current is regulated and the PFC is achieved using the control diagram in Fig. 6, where the LED current feedback loop is highlighted. The change of compensation signal $v_{\text{comp\_}p}$ at primary side can lead to the change of rms input current, thereafter results in the input power change and the dc output voltage (V_{LED}) change. The LED current (I_{LED}) is controlled by changing the dc component in the output voltage (V_{LED}). With a PFC controller, the LED current (I_{LED}) is regulated exactly equal to its reference by controlling the output voltage (V_{LED}).

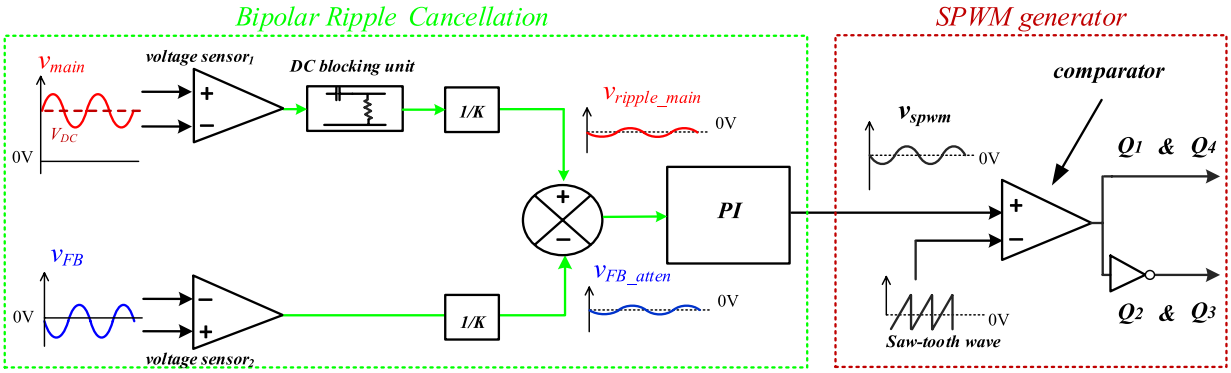


Fig. 5. Control block diagram of bipolar ripple cancellation.

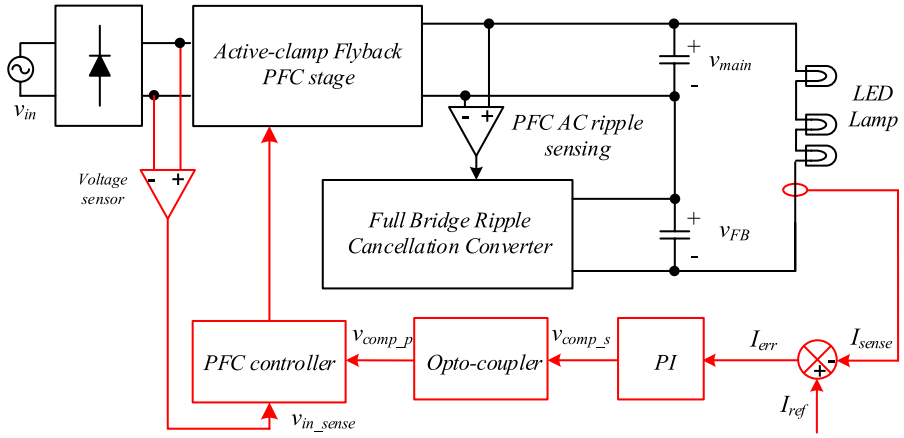


Fig. 6. LED current regulation and PFC.

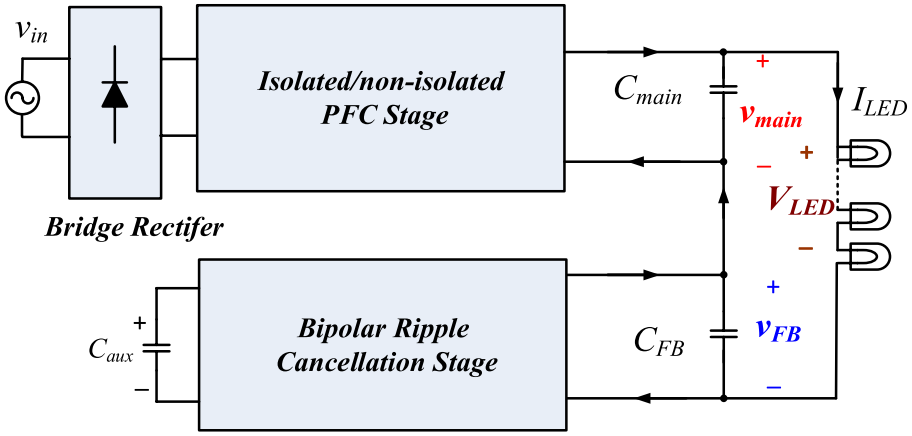


Fig. 7. Block diagram of the proposed electrolytic-capacitor-less LED driver with floating capacitor bipolar ripple cancellation stage.

In fact, the FB RCC does not affect the average value of V_{LED} and I_{LED} and only cancels the double line frequency ac component in the LED voltage. In this way, the LED voltage can be a pure dc voltage using the FB RCC. At the same time, unity input PF can be achieved by flyback converter at the primary side.

III. Bipolar Ripple Cancellation Method Using Floating Capacitor

In the above circuit, an additional winding is added from the main transformer to provide the auxiliary voltage as the input of the FB RCC. This increases the circuit complexity and costs a little bit. It is noted, however, that a floating capacitor can be used as the input of the full-bridge converter because the net power provided by the full-bridge converter is zero under ideal condition and very small if the power loss in the FB RCC is considered. The voltage of the floating capacitor can be regulated by a slow voltage control loop.

Fig. 7 shows the block diagram of the proposed LED driver configuration with floating capacitor FB RCC. It is noted that this improved bipolar ripple cancellation configuration is suitable for both isolated and nonisolated single-stage PFC topologies.

Since the high-power LED bulbs usually require electrical isolation, the isolated flyback topology is still used as the PFC stage to demonstrate the power structure. The architecture

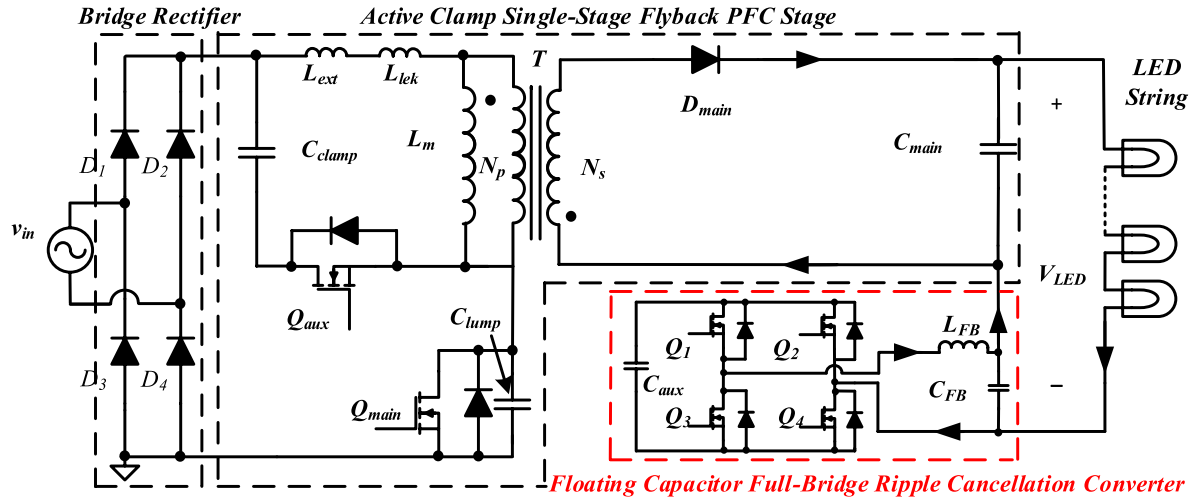


Fig. 8. Realization of proposed electrolytic-capacitor-less LED driver architecture with combined control strategy.

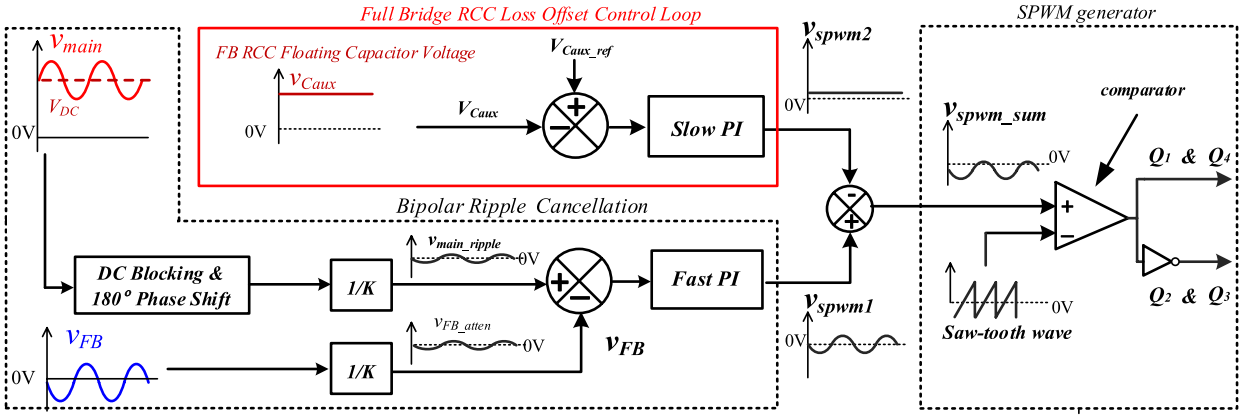


Fig. 9. Bipolar ripple cancellation control strategy.

of the LED driver with the proposed floating capacitor FB RCC is shown in Fig. 8. The FB RCC is still comprised of four switches (Q_1~Q_4), one inductor (L_{FB}) and two capacitors (input capacitor C_{aux} and output capacitor C_{FB}). It is noticed that voltage across C_{aux} (v_{Caux}) in this bipolar ripple cancellation stage contains 120-Hz ripple while C_{FB} only filters out the high switching-frequency noise as a part of output filter. Therefore, the C_{FB} is of a quite small value (<5 μF). The detailed C_{aux} design equations are given in Section III-C.

The complete control block diagram of the improved ripple cancellation converter is shown in Fig. 9. The basic ac ripple cancellation control blocks are shown in Fig. 9 (dotted black boxes). The basic ripple cancellation control processes have already been elaborated in Section II-B, which must feature a high bandwidth to provide a quick ac reference tracking ability.

The significant difference between the control strategies of the two proposed power structures (between Figs. 4 and 8) lies in the method to offset the power loss in the FB RCC. In order to ensure a good ripple cancellation ability of the proposed floating capacitor FB RCC, a power loss offset loop is added to the basic bipolar ripple cancellation loop, which is highlighted in Fig. 9 (red box), where the FB RCC floating capacitor voltage (v_{Caux}) is regulated through a slow PI control loop. This extra control helps to avoid the under-cancellation phenomenon described as follows.

A. Under-Cancellation Phenomenon and V_{Caux} Regulation

When the voltage of the main output is higher than the LED dc output voltage, the FB RCC will provide a negative voltage to cancel the ripple and the energy will flow into the FB RCC. When the voltage of the main output is lower than the LED dc output voltage, the FB RCC will provide a positive voltage to cancel the ripple and the energy will flow out of the FB RCC. If the FB RCC is lossless, the sum of the input energy and the output energy in a half-line cycle will be equal, and thus the C_{aux} voltage will be self-balancing and v_{FB} presents a symmetrical ac curve, as shown in Fig. 10(a). In this case, the FB RCC provides a pure ac voltage with zero dc bias, which is identical with the case when the cancellation loss is offset via the secondary transformer winding, as shown in Fig. 3.

However, the FB RCC has power loss in practical implementation. If the C_{aux} voltage is not regulated and there is no loss offset mechanism, the input energy to the full-bridge

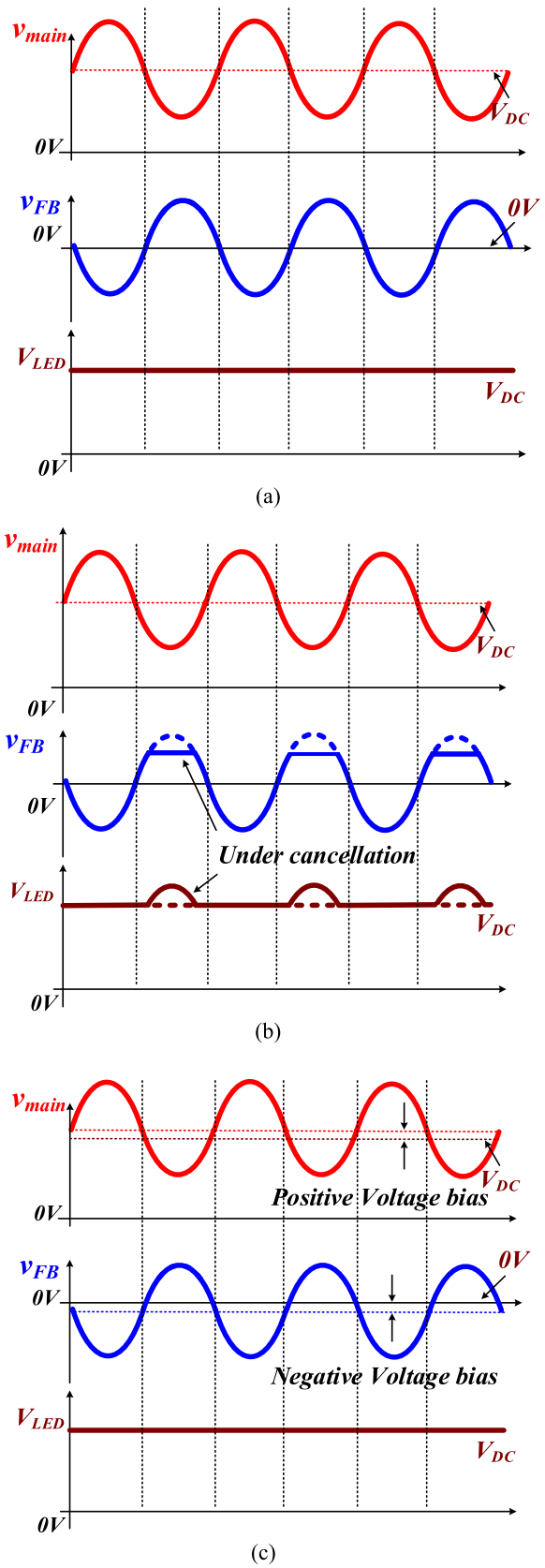


Fig. 10. Under-cancellation phenomenon analysis. (a) Ideal case. (b) Without loss offset loop. (c) With proposed loss offset loop.

RCC stage will be less than the output energy in a half-line cycle, then the C_{aux} will be discharged and the C_{aux} voltage will drop. When the C_{aux} voltage is sufficiently low, the FB RCC can no longer produce the peak voltage required to cancel the main stage's ripple at valley points, and then under-cancellation may occur. This phenomenon is shown in Fig. 10(b), where periodical bumps occur on top of dc LED voltage at double line frequency.

To solve this problem, the average C_{aux} voltage must be regulated, as shown in Fig. 9 (red box). This loop allows the FB RCC to absorb slightly more input energy than the output energy in each double line frequency cycle in order to offset the energy loss. As a result, the C_{aux} voltage can be kept stable and its average value can be regulated at the reference value ($V_{\text{Caux\_ref}}$). According to the electrical features of FB RCC topology, inequality (6) must be satisfied to achieve the fully ripple cancellation

$$v_{\text{Caux}} \geq V_{\text{FB\_pk}} = \frac{1}{2} V_{\text{ripple}} \tag{6}$$

where v_{Caux} is the C_{aux} voltage which contains a 120-Hz voltage ripple component on the top of its average dc voltage. The $V_{\text{FB\_pk}}$ is the peak value of the FB RCC output voltage (v_{FB}), which is decided by the PFC output voltage ripple, V_{ripple}.

B. Combined Control Strategy

In order to accommodate both feedback loops in the floating capacitor FB RCC controller to handles the following two tasks, separately: 1) tracking the shape and magnitude of the periodic ac ripple and 2) compensating the auxiliary stage loss, a combined bipolar ripple cancellation control strategy is proposed, which is shown in Fig. 9.

This control strategy is under the assumption that the FB RCC loss changes quite slow so that it can be considered as a dc value in one half-line cycle, which is practical for a fixed-load LED driver.

As shown in Fig. 9, the fast PI loop tracks the ac ripple reference ($v_{\text{ripple\_main}}$) and provides an ideal Sinusoidal Pulse Width Modulation (SPWM) control output (v_{spwm1}), while the slow PI loop regulates the floating capacitor voltage (V_{Caux}), which generates a dc control voltage (v_{spwm2}). These two controlling outputs are added together as $v_{\text{spwm\_sum}}$ and then compared with the sawtooth wave to generate the SPWM driver signals for the four switches in FB RCC. As a result, FB RCC outputs a reversed ac voltage ripple with a very small negative dc voltage bias, as shown in Fig. 10(c).

It should be noticed that this negative dc voltage bias in the FB RCC output (v_{FB}) will not affect ac ripple reference ($v_{\text{ripple\_main}}$) and the normal operation of the fast loop in the basic bipolar ripple cancellation because this is a dc signal (according to the assumption). All the dc information existing in the PFC output is blocked by the analog differential circuit before it becomes the reference for the fast loop. Therefore, the reference signals of these two loops are decoupled and both loops are able to operate stably and simultaneously.

C. FB RCC Input Capacitor C_{aux} Design

In order to avoid the under-cancellation phenomenon as shown in Fig. 10(b), the C_{aux} value is critical. Its voltage

changes periodically at double line frequency, corresponding to energy exchanging inside the FB RCC. The design should ensure that the voltage across C_{aux} is always higher than the auxiliary output voltage, v_{FB}, at any time instant.

Under the assumption that FB RCC is operating at switching frequency much higher than the double line frequency, ($f_{\text{sw}} \gg 2 \times f_{\text{line}}$), the C_{aux} capacitance value is designed by the LED current (I_{LED}), the ac line voltage frequency (f_{line}), the allowed input voltage ripple ($V_{\text{Caux\_ripple}}$), the average input voltage ($V_{\text{Caux\_avg}}$), as well as the pk-to-pk output voltage of FB RCC (V_{ripple}). The expression is shown in

$$C_{\text{aux}} \geq \frac{I_{\text{LED}} \cdot V_{\text{ripple}}}{4\pi \cdot f_{\text{line}} \cdot V_{\text{Caux\_avg}} \cdot V_{\text{Caux\_ripple}}}. \tag{7}$$

The capacitor C_{aux} selected based on (7) ensures that the FB RCC output completely cancels the ripple component in LED lamp current, I_{LED}. The detailed derivation is shown in the Appendix.

IV. Step-by-Step Design Procedure for Bipolar Ripple Cancellation Converter

In light of the analysis discussed above, the design procedure of the proposed LED driver with bipolar ripple cancellation stage (FB RCC) is summarized as follows.

A. Selection of Voltage Rating of the FB RCC Input Capacitor C_{aux}

Multilayer ceramic capacitor is a good choice for the FB RCC input capacitor due to its small size and low cost as compared with the film capacitor [33], [34]. However, high-capacitance ceramic capacitors (>10 μF) become expensive or even unavailable when the required dc voltage rating is over 50 V. Therefore, the design limitation of 50 V C_{aux} voltage rating is used in the practical design. The FB RCC switch ratings and the allowable PFC voltage ripple can be decided accordingly.

B. Selection of the FB RCC MOSFETs and Design the Cancellation Stage

The voltage stress of the full-bridge switches is the voltage across C_{aux} and is, therefore, <50 V, as discussed above. In order to reduce losses, MOSFETs with a low drain-to-source voltage V_{ds}, low $R_{\text{ds(ON)}}$, and low total gate charge, Q_g, are preferred. In the experimental prototype, MOSFETs with voltage rating of 30 V are used. The parameters and rating values of the full-bridge output inductor (L_{FB}) and output capacitor (C_{FB}) are selected as 47 μH and 4.7 μF 50 V.

C. Selection of PFC Stage Output Capacitance

The following three points must be taken into consideration when selecting the optimal PFC output capacitance.

1) The peak voltage of the double line frequency ripple should be limited to be less than the average output voltage of the LED load to ensure a high PF for the PFC stage, as per

$$\frac{1}{2} V_{\text{ripple}} \leq V_{\text{LED}}. \tag{8}$$

TABLE I
Specifications of LED Driver

V_{in}	V_{LED}	I_{LED}	P_O	f_{line}
85~265 Vac	≈150 Vdc	0.7A	100 W	60 Hz

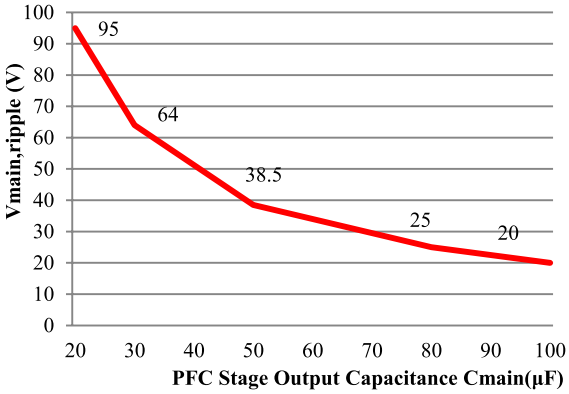


Fig. 11. PFC output capacitance versus PFC output pk–pk ripple voltage with LED current of 0.7 A.

2) Although the double line frequency component is removed from the LED output current by the bipolar ripple cancellation stage, a high switching-frequency component is introduced. A higher PFC output capacitance helps to dampen this high-frequency component.
3) C_{main} serves as an energy storage component in the main stage to buffer the power difference and mitigate the load current ripple. V_{ripple} is inversely proportional to C_{main}, according to (5). Minimizing the PFC output capacitance and limiting the double line frequency voltage ripple is a tradeoff, which affects the maximum voltage stress on the PFC output capacitor as expressed in (9) and the voltage stress on the switches in the FB RCC, which is discussed in Section V

$$V_{\text{main\_pk}} = V_{\text{LED}} + \frac{1}{2} V_{\text{ripple}}. \tag{9}$$

With these factors in mind, the LED driver experimental prototype has been designed to meet the following the specifications, as shown in Table I.

With the specified LED current, the amplitude of 120-Hz ripple of PFC voltage depends on the output capacitance value, according to (5). It increases dramatically when the output capacitance is less than 100 μF, as shown in Fig. 11.

The pk-to-pk ripple voltage goes to 40 V (the peak value is 20 V) when the output capacitance is set as 44 μF. In the experimental prototype, two 22-μF parallel film capacitors are used and the 120-Hz ripple is ~40 V pk-to-pk. The maximum PFC output voltage of PFC is 150 + 20 = 170 V (<250 V capacitor voltage rating).

D. Design of FB RCC Input Capacitor C_{aux}

In order to satisfy the inequality (6), the average value of the input capacitor voltage, $V_{\text{Caux\_avg}}$, is selected as 35 V with a maximum 10 V pk-to-pk ripple, $V_{\text{Caux\_ripple}}$. So that the

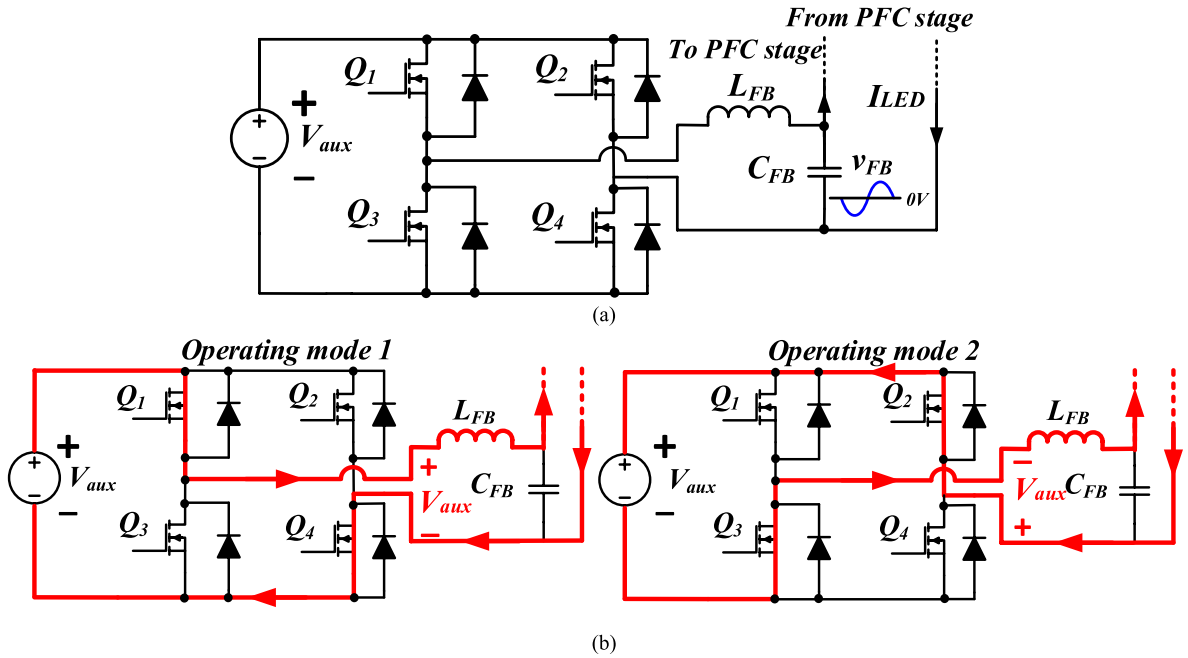


Fig. 12. Operating modes of bipolar ripple cancellation converter. (a) Stage prototype. (b) Operation modes.

TABLE II
C_{aux} DESIGN PARAMETERS

T_{sw}	V_{FB_pk}	V_{Caux_avg}	V_{Caux_ripple}
1/156kHz	20V	35V	10V (peak-peak)

allowed minimum input voltage is 30 V which is a reasonable value to ensure the normal bipolar ripple cancellation operation of the FB RCC. All the parameters for C_{aux} design are listed in Table II.

Substitution of the values in Table II into (7) yields a minimal requirement ($C_{\text{aux}} \geq 106\ \mu$F) for FB RCC input capacitor value to avoid under-cancellation phenomenon. Therefore, C_{aux} is selected as 120 μF in the prototype (10 μF $\times$ 12 pieces 50 V 1206 ceramic caps).

E. C_{FB} and C_{aux} Layout to Suppress the Audible Noise

A ceramic capacitor expands when a voltage is applied and contracts when the voltage is reduced. The Printed Circuit Board (PCB) flexes as the capacitor changes in size because the ends of the capacitor mechanically couple to the PCB through solder. Applying the voltage ripple at audible frequency makes the PCB operate as a speaker. In the design, both C_{FB} and C_{aux} are processing power flow at 120 Hz. Particular measures have been taken to suppress the audible noise.

In the experimental prototype, there are 12 pieces of ceramic capacitor (10 μF 50 V 1206) connected in parallel as the FB RCC input (floating) capacitors, which are soldered on both sides of the PCB, six on the top layer and six on the bottom layer, back-to-back. In this way, the tension caused by the capacitors at the top side is significant offset by the same tension caused by the ones on the bottom side. Therefore, the audible noise is suppressed. In addition, routing a slot on both sides of the C_{FB} also helps to reduce the noise.

V. ANALYSIS OF PROPOSED BIPOLAR RIPPLE CANCELLATION STAGE

The proposed bipolar ripple cancellation method with FB RCC features a bipolar output (both positive and negative voltages), as shown in Fig. 12(a). Two modes of the cancellation circuit are shown in Fig. 12(b).

Since the RCC's output current is the LED current (a dc current), from a power flow point of view, the RCC stage is different from the traditional single-phase full-bridge inverter in that the circuit does not contribute dc power to the LED load. It instead acts as a reservoir to buffer the power difference and completes an exchange of instantaneous power with the load once every half of a line cycle. The power loss of the bipolar ripple cancellation stage is offset either via an auxiliary winding from the main PFC stage (using the basic bipolar control strategy in Section II-B) or from the output side of FB RCC using floating capacitor (using the improved control strategy in Section III-B), so that the input voltage of the FB RCC is always higher than its output voltage and the cancellation can be committed normally. The proposed bipolar ripple cancellation methods (with FB RCC) provide the following advantages.

A. Low-Voltage-Rating Components in the Cancellation Stage

The four MOSFETs $Q_1 \sim Q_4$ conduct diagonally to provide paths for the output current I_{LED}, as shown in Fig. 12(b). According to the electrical features of FB RCC topology, it sees the component stress equal to half of the double line frequency ripple, shown in

$$V_{\text{FB,max}} \geq \frac{1}{2} V_{\text{ripple}} \tag{10}$$

where $V_{\text{FB,max}}$ is the switches' voltage stress in the FB RCC.

Therefore, the proposed bipolar ripple cancellation method presents a double voltage ripple cancellation ability (given the components voltage stress in the additional stage are the same), compared with the existing unipolar cancellation method in [24]–[26], which is more beneficial for high-power high-voltage LED driver applications, where low cost of auxiliary circuits are required.

B. Applicable for Both Isolated and Nonisolated PFC Topologies

With the help of an extra voltage regulation loop, the cancellation stage loss is offset from the output side of the FB RCC. Therefore, no auxiliary winding is required for the improved FB RCC with a floating capacitor, making it a more cost-effective and more flexible solution applicable for both isolated and nonisolated LED driver applications.

C. Suitable for Variable-Output-Voltage LED Drivers

In order to adept different LED-load combinations, customers require the drivers to handle a wide output voltage range under the rated output current. The ratio of the highest specification over the lowest specification is usually higher than two times (e.g., $V_{\rm LED} = 60$–150 V). With the existing cancellation technologies proposed in [17], [18], and [28], given the auxiliary winding turn ratio is fixed, the component voltage rating has to be overdesigned under the low output voltage operation (e.g., $V_{\rm LED} < 150$ V) to fit the voltage stress at the highest output voltage operation (e.g., $V_{\rm LED} = 150$ V), resulting a nonoptimal solution.

As to the second proposed floating capacitor ripple cancellation method (given in Section VI), the minimal $C_{\rm aux}$ voltage of FB RCC, $v_{\rm Caux}$, should be larger than the peak ripple voltage at the main output, 0.5 $V_{\rm ripple}$ (by ~10%) to ensure the full cancellation of the double line frequency voltage ripple, according to (6).

Equation (5) shows that the pk-to-pk value of the double line frequency voltage ripple in PFC output, $V_{\rm ripple}$, is only proportional to the LED output current I_{LED} as well as the PFC output capacitance $C_{\rm main}$, given the line frequency $f_{\rm line}$ is fixed. Therefore, the voltage stress of the floating capacitor ($C_{\rm aux}$) is designed based on the highest LED current $I_{\rm LED}$ as the worst case (in this paper, 0.7 A is the rated load current).

Compared with the existing cancellation technologies proposed in [24]–[26] as well as the first proposed ripple cancellation method (given in Section III in this paper) where the input capacitor voltage is decided by the LED driver dc output voltage (because the input capacitor is connected by an auxiliary winding from the PFC stage), the second proposed floating capacitor FB RCC features significantly reduced component voltage stress and energy loss. As a result, this improved bipolar ripple cancellation method solves the existing overdesigning problem on the component voltage rating in FB RCC at low output voltage operation for variable-output-voltage LED drivers and saves the components' cost in the auxiliary circuits.

TABLE III
PROTOTYPE PARAMETERS VALUES

Active Clamp Single-stage Flyback PFC Stage	
Output Capacitor (C_{main})	44 μF (22 μF×2, 250V Film Caps)
Switches (Q_{main} Q_{aux})	SPP11N80C3
Diode (D_{main})	C3D16060
Turns Ratio (N_p:N_{s1}:N_{s2})	6:5:1 or 6:5:0 (no auxiliary winding for the RCC with floating capacitor)
Magnetizing Inductance (L_m)	1300 μH
Leakage Inductance (L_{lek})	33 μH
External Leakage Inductor (L_{ext})	15 μH
Active Clamp Capacitor (C_{clamp})	272 nF (68 nF×4, 400V Film Caps)
Single-stage PFC Controller	NCP1652A
Bipolar FB RCC Stage	
Switching Frequency (f_{sw})	156 KHz
Input Capacitor (C_{aux})	120 μF (10 μF×12, 50V 1206 Ceramic Caps)
Output Inductor (L_{FB})	47 μH
Output Capacitor (C_{FB})	4.7 μF (50V 1206 Ceramic Cap)
Full-bridge Switches (Q_1~Q_4)	TPN11003NLLQ×4 (30V, 11mΩ)
SPWM Controller	MC33060A
LED lamp Load	
LED Chip Part Number	XMLEZW-02-0000-0B00T527F×27 connected in series
Forward Voltage/pcs (V_f) Typ	6 V
Max Current (I_{max})	2 A
Luminous Flux/pcs @ 700 mA	270 lm

D. High Efficiency

The bipolar ripple cancellation method also yields a high efficiency, since the FB RCC does not contribute dc power to the LED load. Without the auxiliary winding, the second proposed bipolar ripple cancellation method presents even higher efficiency benefiting from saving the loss in the auxiliary winding (N_{s2}) and diode ($D_{\rm aux}$), shown in Fig. 4. This will be demonstrated in the experimental result.

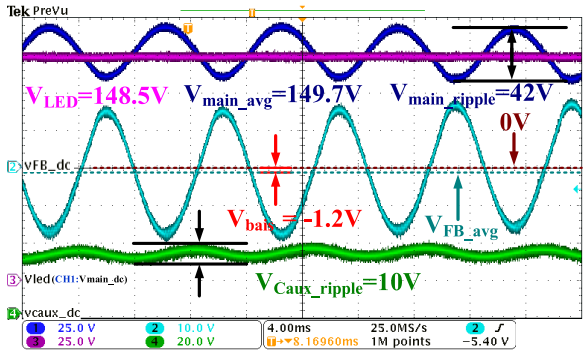
VI. EXPERIMENTAL VERIFICATION

A 100-W CCM single-stage flyback LED driver with bipolar ripple cancellation stage has been built. Following the proposed design procedure in Section IV-C results in the PFC output capacitance to be 44 μF, and thus the 120-Hz ripple of the PFC output voltage is 40 V (pk-to-pk). Therefore, the peak value of FB RCC output is 20 V (peak), and $C_{\rm aux}$ has been selected as 120 μF in the prototype so that the 120-Hz voltage ripple in $v_{\rm Caux}$ is limited to 5 V (peak) when its average voltage is regulated at 35 V. The minimum voltage across $C_{\rm aux}$ is 30 V.

The design specifications are given in Table I, while the detailed prototype parameters are shown in Table III.

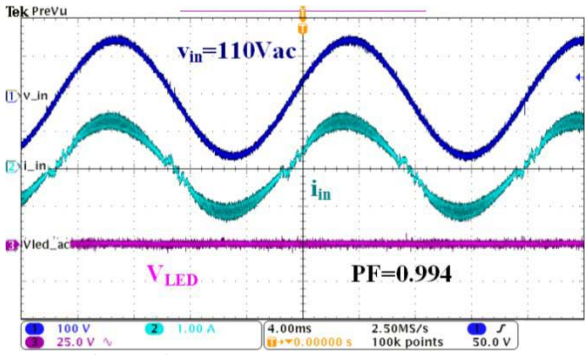
A. Floating Capacitor Voltage Regulation Performance

Fig. 13 shows the key experimental waveforms of the floating capacitor FB RCC (when $V_{\rm in} = 110$ $V_{\rm ac}$, $V_{\rm LED} \approx 150$ V,



CH1:DC coupled PFC stage output voltage (v_{main})
CH2: DC coupled FB RCC output voltage (v_{FB})
CH3: DC coupled LED lamp voltage (V_{LED})
CH4: DC coupled FB RCC floating capacitor voltage (vCaux)

Fig. 13. Key experimental waveforms of floating capacitor FB RCC, when $V_{\text{in}} = 110$ V_{ac}, $V_{\text{LED}} \approx 150$ V, $I_{\text{LED}} = 0.7$ A, and $P_O = 100$ W.



CH1: AC input voltage (v_{in})
CH2: AC input current (i_{in})
CH3: AC coupled LED lamp voltage (V_{LED})

Fig. 14. Input current and output voltage of the proposed LED driver, when $V_{\text{in}} = 110$ V_{ac}, $V_{\text{LED}} \approx 150$ V, $I_{\text{LED}} = 0.7$ A, and $P_O = 100$ W.

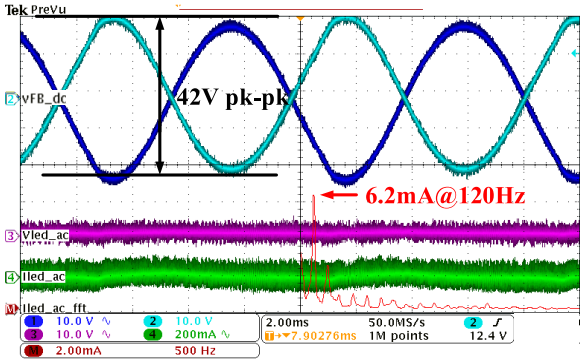
$I_{\text{LED}} = 0.7$ A, and $P_O = 100$ W), in which the floating capacitor voltage v_{Caux} is shown in CH4 (dc coupled). After 120-μF ceramic capacitors are used as the FB RCC floating capacitor, v_{Caux} is regulated at 35 ± 5 V as expected in Table II by the proposed loss offset loop.

Besides, the PFC stage output voltage (v_{main}) is shown in CH1 (dc coupled), whose average value ($V_{\text{main\_ripple}}$) is 149.7 V. The FB RCC output voltage (v_{FB}) is shown in CH2 (dc coupled), whose average voltage ($V_{\text{FB\_avg}}$) has a small negative dc voltage bias of -1.2 V. As a result, a dc voltage (V_{LED}) of 148.5 V (149.7 V $-$ 1.2 V $=$ 148.5 V) is obtained and is applied to the LED lamp to produce dc LED current, as shown in CH3 (dc coupled). This 1.2 V voltage bias is caused by the energy loss in the floating capacitor FB RCC and the loss can be calculated using the measured voltage bias value ($P_{\text{loss}} = V_{\text{bias}} \times I_{\text{LED}} = 1.2$ V $\times$ 0.7 A $= 0.84$ W).

Fig. 14 shows the input voltage and input current waveform of proposed bipolar ripple cancellation method ($v_{\text{in}} = 110$ V_{ac}), which has achieved a high PF of 0.994.

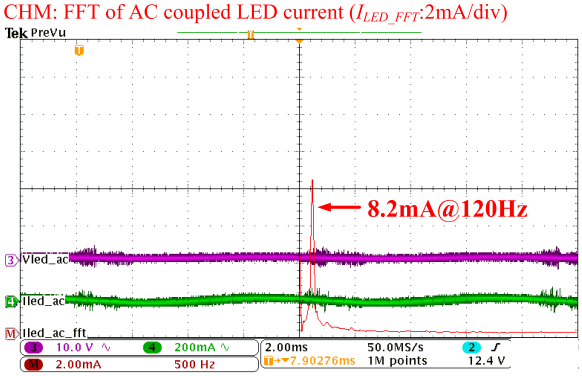
B. Current Ripple Cancellation Performance

Both the two power structures of FB RCC have been verified with a single-stage flyback PFC stage (main stage)



(a)

CH1: AC coupled PFC stage output voltage (v_{main}:10V/div)
CH2: FB RCC output voltage (v_{FB}:10V/div)
CH3: AC coupled LED lamp voltage (V_{LED}:10V/div)
CH4: AC coupled LED lamp current (I_{LED}:200mA/div)
CHM: FFT of AC coupled LED current (I_{LED_FFT}:2mA/div)

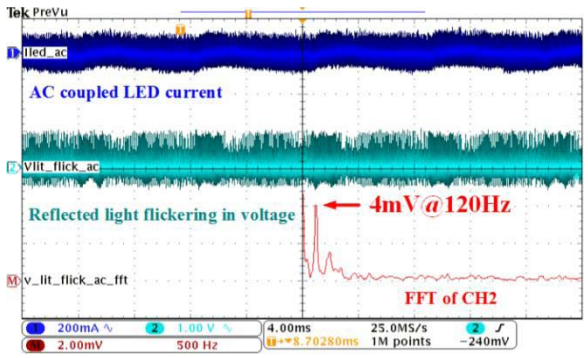


(b)

CH1: AC coupled PFC stage output voltage (v_{main}:10V/div)
CH2: FB RCC output voltage (v_{FB}:10V/div)
CH3: AC coupled LED lamp voltage (V_{LED}:10V/div)
CH4: AC coupled LED lamp current (I_{LED}:200mA/div)
CHM: FFT of AC coupled LED current (I_{LED_FFT}:2mA/div)

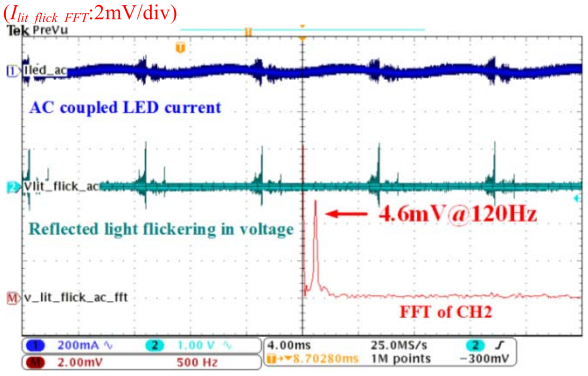
Fig. 15. Ripple cancellation performance of the proposed LED driver, when $V_{\text{in}} = 110$ V_{ac}, $V_{\text{LED}} \approx 150$ V, $I_{\text{LED}} = 0.7$ A, and $P_o = 100$ W. (a) LED driver with the proposed FB RCC ($C_{\text{main}} = 44$ μF, $C_{\text{aux}} = 120$ μF, and $C_{\text{FB}} = 4.7$ μF). (b) Active-clamp single-stage flyback LED driver ($C_o = 4700$ μF).

and present the same ripple cancellation performance. The key waveforms of the proposed LED driver configuration with only 48.7-μF total output capacitance ($C_{\text{main}} + C_{\text{FB}}$) is shown in Fig. 15(a) whose reference polarity is the same in Fig. 3. The ac voltage generated by the FB RCC (CH2, ac coupled) mitigates the 120-Hz PFC ripple (CH1, ac coupled), resulting in a total flat voltage (CH3, ac coupled) and flat LED current (CH4, ac coupled), the current ripple value at 120 Hz is shown in fast Fourier transform (FFT) Mathematical Channel of the scope (CHM). The 120-Hz PFC voltage ripple is 42 V pk–pk before cancellation. The LED output current ripple at 120 Hz is 6.2-mA rms after cancellation. According to (5), when using the conventional single-stage LED drivers, such a small voltage ripple can be only achieved when the output capacitance is increased to 4700 μF. Fig. 15(b) shows the output voltage and LED current of a single-stage LED driver under 4700-μF output capacitance with the same power train parameters, the 120-Hz current ripple value is 8.2 mA. It is evident that the proposed solution reduces the output capacitance value by 99%! In addition, it should be noticed that only 44-μF C_{main} is of



(a)

CH1: AC coupled LED current (I_{LED}:200mA/div)
CH2: AC coupled reflected light flickering in voltage (v_{lit_flick}:1V/div)
CHM: FFT of reflected light flickering in voltage ($I_{lit\_flick\_FFT}$:2mV/div)



(b)

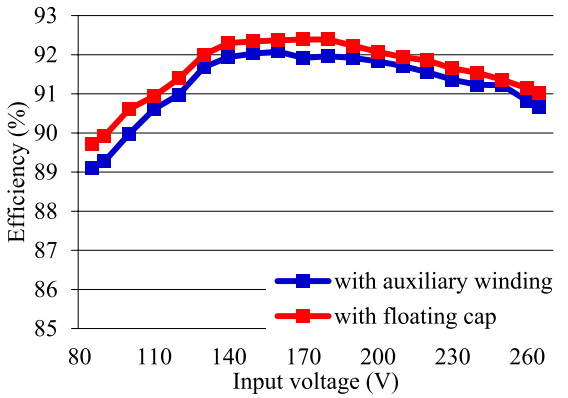
CH1: AC coupled LED current (I_{LED}:200mA/div)
CH2: AC coupled reflected light flickering in voltage (v_{lit_flick}:1V/div)
CHM: FFT of reflected light flickering in voltage ($I_{lit\_flick\_FFT}$:2mV/div)

Fig. 16. Light flickering reduction performance comparison, when V_{in} = 110 Vac, V_{LED} ≈ 150 V, I_{LED} = 0.7 A, and P_o = 100 W. (a) LED driver with the proposed bipolar ripple cancellation (C_{main} = 44 μF, C_{aux} = 120 μF, and C_{FB} = 4.7 μF). (b) Active-clamp single-stage flyback LED driver (C_o = 4700 μF).

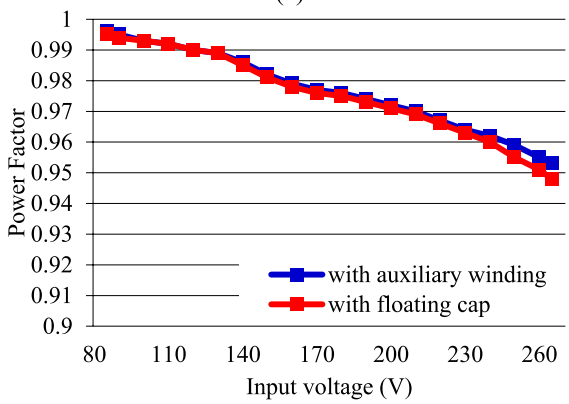
high rating (voltage stress is 250 V) while both C_{FB} and C_{aux} are low-voltage-rating components (voltage stress is 50 V).

C. Light Flickering Comparison

A luminance to voltage conversion device was built to measure the light flickering performance of the proposed bipolar ripple cancellation method. Fig. 16 shows the lighting fluctuation comparison between the LED lamps driven by the proposed LED driver in Fig. 16(a) and the conventional single-stage active-clamp flyback LED driver in Fig. 16(b). In order to highlight the 120-Hz component of the signals, both CH1 and CH2 in Fig. 16 are ac coupled. As a result, only a small dc component remains in the mathematical channel, as shown in the most left part FFT signal. The proposed LED driver with bipolar ripple cancellation shows the superior light flickering reduction ability (4-mV reflected light flickering in voltage) over the conventional LED driver with 4700-μF output capacitance (4.6-mV reflected light flickering in voltage).



(a)



(b)

Fig. 17. Performance comparison of the proposed LED drivers when C_{main} = 44 μF, V_{LED} ≈ 150 V, I_{LED} = 0.7 A, and P_o = 100 W. (a) System efficiency. (b) PF.

D. Power Efficiency and Power Factor Performance

Since the proposed FB RCC only processes the ac ripple component, the efficiency loss during ripple cancellation is minimal. In Fig. 17(a) and (b), both the power efficiency and PF performances of the two different bipolar ripple cancellation power structures (blue lines are with auxiliary winding and the red lines are with a floating capacitor) are measured.

The experimental results show that both of the two bipolar ripple cancellation power configurations have exceeded 90.6% power efficiency and 0.97 PF given a universal ac input (110–220 V). The peak efficiency of the system is 92% for the winding-connect bipolar ripple cancellation and 92.5% for the improved bipolar ripple cancellation with floating capacitor. In general, the floating capacitor bipolar ripple cancellation method presents a slightly higher efficiency than the one with auxiliary winding by 0.5%. This slight difference is caused by the loss in extra winding (N_{s2}) and the diode (D_{aux}) from the main PFC stage. As shown in Fig. 18, the power loss contributed by the cancellation stage is generally very small for both the proposed bipolar ripple cancellation structures (<1.4 W). Compared with the major benefit of capacitor value reduction and using film capacitors, the loss is insignificant.

Fig. 19 shows that the experimental prototype has passed IEC61000-3-2 Class C requirements with large margin,

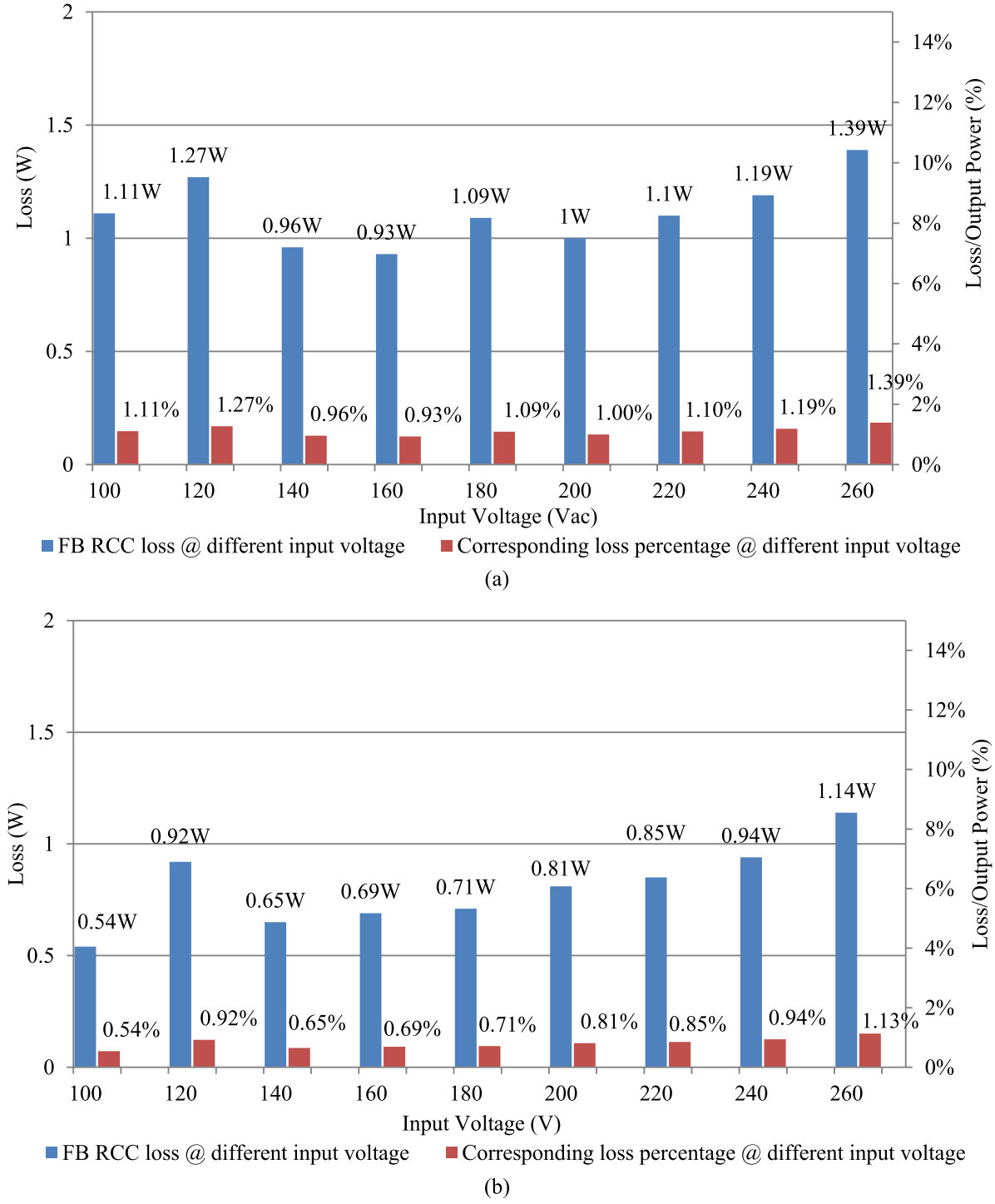


Fig. 18. FB RCC loss performance, when $C_{\text{main}} = 44\ \mu\text{F}$, $V_{\text{LED}} \approx 150$ V, $I_{\text{LED}} = 0.7$ A, and $P_o = 100$ W. (a) With auxiliary winding. (b) With floating capacitor.

because the proposed bipolar ripple cancellation stage (FB RCC) does not affect the original PF performance of the main PFC stage in the LED driver.

E. Prototype Board

Fig. 20(a) shows a photo of the whole prototype board on which both of the proposed control strategies are implemented. The prototype is composed of two parts: 1) the single-stage active clamp PFC stage (main stage) is at the left side of the board and 2) the bipolar ripple cancellation stage (FB RCC) is at the right side. With the bulky PFC output electrolytic capacitors being substituted by the film capacitors as shown in the red box, the whole prototype achieves electrolytic-capacitor-free.

The LED load lamp is made of 27 LED chips from Cree (XMLEZW-02-0000-0B00T527F) connected in series. Fig. 20(b) shows a photo of the LED lamp load used in the experiment.

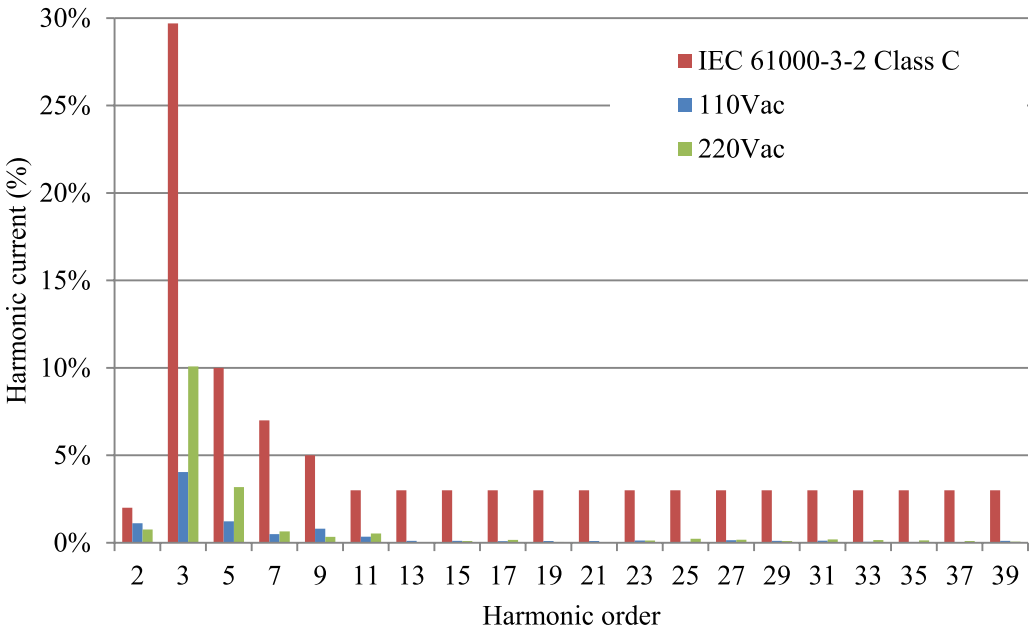
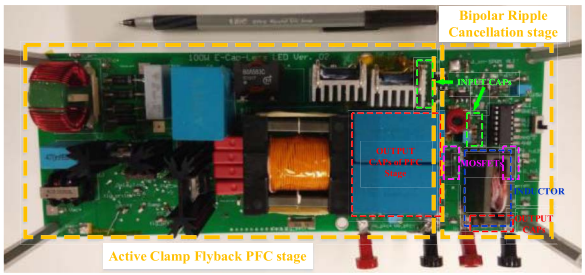
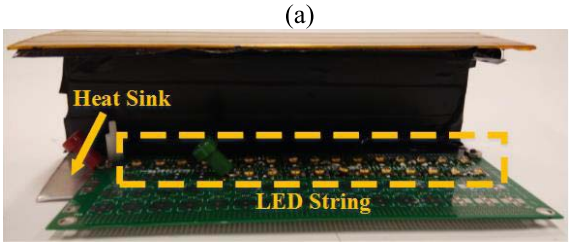


Fig. 19. Harmonic performance at nominal input voltage.



(a)



(b)

Fig. 20. Prototype photos. (a) Proposed LED driver. (b) LED lamp.

VII. Conclusion

This paper has proposed a new high-power LED driver configuration with a bipolar ripple cancellation stage (FB RCC). This cancellation circuit neither impacts the dc output current nor degrades the PF, compensating only the ac ripple at the PFC output. Two different power structures have been proposed. As a result, the required output capacitor value is significantly reduced and the electrolytic capacitors can be replaced by long-life power film capacitors.

Compared with the existing series ripple cancellation configurations in [24]–[26], the proposed configuration features: 1) a double voltage ripple cancellation ability (given the components voltage stress in the additional stage are the same, which is more suitable for high output power and high output voltage applications and 2) a high efficiency comparable with the conventional single-stage solutions.

By innovatively controlling the power flow of the FB RCC, the auxiliary winding can be eliminated, rendering a more cost effective, and more flexible solution for both isolated and nonisolated LED driver applications, which provides the fourth attractive characteristic that the FB RCC input voltage can be regulated separately from the main PFC stage output voltage, avoiding the overdesigning of the component voltage rating in the cancellation stage at low output voltage operation for the variable-output-voltage LED drivers.

A 100 W (150 V/0.7 A) experimental prototype was built. The experimental results demonstrate that, using a 44-μF output capacitor, the double line frequency LED ripple current can be as low as 6.2-mA rms in the proposed configuration, which would otherwise require over 4700-μF output capacitance using conventional single-stage LED drivers.

Appendix

A. FB RCC Floating Capacitor C_{aux} Design Rule Derivation

The instant C_{aux} input voltage is composed of a dc average voltage and a changing double-line-frequency voltage ripple resulting from the charging and discharging of the capacitor by the LED current I_{LED}

$$v_{C_{\text{aux}}} = V_{\text{Caux\_avg}} + v_{\text{Caux\_ripple}}. \tag{11}$$

According to the operation modes of ripple cancellation stage, the input capacitor is charged when Q_2 and Q_3 are conducted (Q_1 and Q_4 are OFF) and it is discharged when Q_1 and Q_4 are conducted (Q_2 and Q_3 are OFF). These two intervals are shown in the following equations, separately:

$$T_{\text{charge}} = T_{\text{sw}} \cdot (1 - D) \tag{12}$$

$$T_{\text{discharge}} = T_{\text{sw}} \cdot D \tag{13}$$

where T_{sw} is the switching period of cancellation stage. D is the duty cycle of the driving signals for Q_1 and Q_4, shown

in the following equation:

$$D(t) = \frac{1}{2} + \frac{1}{2} \cdot M \cdot \sin(2\omega t) \tag{14}$$

where ω is angular frequency of line voltage and M is the modulation index of SPWM, expressed as

$$M = \frac{\frac{1}{2} V_{\text{ripple}}}{V_{\text{Caux\_avg}}}. \tag{15}$$

Since the average current going through the switches is fixed by the load, the difference between charging time and discharging time of each switching cycle determines the behavior of input current, leading to the increase or decrease of the input voltage. The charge for each cycle can be expressed by the following equation:

$$\begin{aligned} Q_{\text{discharge}}(t) &= I_{\text{LED}} \cdot (T_{\text{discharge}}(t) - T_{\text{charge}}(t)) \\ &= I_{\text{LED}} \cdot T_{\text{sw}} \cdot M \cdot \sin(2\omega t). \end{aligned} \tag{16}$$

The sum of discharge is expressed in the following equation:

$$\begin{aligned} Q_{\text{discharge\_sum}}(nT_{\text{sw}}) &= \sum_{t=0}^{nT_{\text{sw}}} Q_{\text{discharge}}(t) \\ &= \sum_{k=1}^{n} I_{\text{LED}} \cdot T_{\text{sw}} \cdot M \cdot \sin(2\omega \cdot kT_{\text{sw}}). \end{aligned} \tag{17}$$

According to the characteristics of the two-level SPWM modulation strategy, the discharging period is always longer than the charging time during the first half-line cycle before it enters the other half-line cycle. Therefore, the input capacitor keeps discharging over each switching cycle and the voltage keeps decreasing until it touches the valley at the half cycle point. Then, the biggest voltage drop can be calculated in the following equation:

$$V_{\text{Caux\_ripple}} = \frac{Q_{\text{discharge\_sum}}\left(\frac{T_{\text{line}}}{4}\right)}{C_{\text{aux}}}. \tag{18}$$

In fact, this is the worst case because the output voltage is on the peak value simultaneously.

$Q_{\text{discharge\_sum}}(T_{\text{line}}/4)$ in (18) can be simplified into (19) after the mathematical deduction

$$\begin{aligned} Q_{\text{discharge\_sum}}\left(\frac{T_{\text{line}}}{4}\right) &= \sum_{k=1}^{\frac{T_{\text{line}}}{4T_{\text{sw}}}} I_{\text{LED}} \cdot M \cdot T_{\text{sw}} \cdot \sin\left(\frac{4\pi T_{\text{sw}}}{T_{\text{line}}} k\right) \\ &= \frac{I_{\text{LED}} \cdot M \cdot T_{\text{sw}}}{\tan\left(\frac{2\pi T_{\text{sw}}}{T_{\text{line}}}\right)}. \end{aligned} \tag{19}$$

Since $T_{\text{sw}} \ll T_{\text{line}}$ ($f_{\text{sw}} \gg f_{\text{line}}$)

$$\tan\left(\frac{2\pi T_{\text{sw}}}{T_{\text{line}}}\right) \approx \frac{2\pi T_{\text{sw}}}{T_{\text{line}}}. \tag{20}$$

Then, (19) can be further simplified, as shown in

$$Q_{\text{discharge\_sum}}\left(\frac{T_{\text{line}}}{4}\right) = \frac{I_{\text{LED}} \cdot M}{2\pi \cdot f_{\text{line}}} \tag{21}$$

where f_{line} is the ac line voltage frequency.

Therefore, FB RCC is able to work normally for the whole line cycle as long as the input valley voltage is set higher than the peak output voltage. The final floating capacitor C_{aux} design rule is shown in

$$\begin{aligned} C_{\text{aux\_min}} &\geq \frac{Q_{\text{discharge\_sum}}\left(\frac{1}{4}T_{\text{line}}\right)}{V_{\text{Caux\_ripple}}} \\ &= \frac{I_{\text{LED}} \cdot V_{\text{ripple}}}{4\pi \cdot f_{\text{line}} \cdot V_{\text{Caux\_avg}} \cdot V_{\text{Caux\_ripple}}}. \end{aligned} \tag{22}$$

B. FB RCC Floating Capacitor C_{aux} Design Rule Derivation From the Energy Balance Point of View

The energy released from C_{aux} with its voltage change from $V_{\text{Caux\_peak}}$ to $V_{\text{Caux\_valley}}$ can be expressed in the following equation:

$$\begin{aligned} \Delta E &= \frac{1}{2} C_{\text{aux}} \cdot \left(V_{\text{Caux\_peak}}\right)^2 - \frac{1}{2} C_{\text{aux}} \cdot \left(V_{\text{Caux\_valley}}\right)^2 \\ &= C_{\text{aux}} \cdot V_{\text{Caux\_avg}} \cdot V_{\text{Caux\_ripple}}. \end{aligned} \tag{23}$$

The energy delivered to the LED string from the FB RCC during the above period can be calculated as follows:

$$\begin{aligned} W = PT &= \int_0^{\frac{T_{\text{line}}}{4}} v_{\text{CFB}}(t) \cdot I_{\text{LED}}(t) \cdot dt \\ &= I_{\text{LED}} \int_0^{\frac{T_{\text{line}}}{4}} v_{\text{CFB}}(t) \cdot dt \\ &= I_{\text{LED}} \int_0^{\frac{T_{\text{line}}}{4}} V_{\text{ripple}} \cdot \sin(2\pi\ (2f_{\text{line}})\, t) \cdot dt \\ &= \frac{I_{\text{LED}} \cdot V_{\text{ripple}}}{4\pi \cdot f_{\text{line}}}. \end{aligned} \tag{24}$$

Neglecting the energy loss in the FB RCC, the circuit should follow the energy balance rule: $\Delta E = W$. Then

$$C_{\text{aux}} \cdot V_{\text{Caux\_avg}} \cdot V_{\text{Caux\_ripple}} = \frac{I_{\text{LED}} \cdot V_{\text{ripple}}}{4\pi \cdot f_{\text{line}}}. \tag{25}$$

The resulting floating capacitor C_{aux} design rule is the same as that from the first derivation

$$C_{\text{aux\_min}} \geq = \frac{I_{\text{LED}} \cdot V_{\text{ripple}}}{4\pi \cdot f_{\text{line}} \cdot V_{\text{Caux\_avg}} \cdot V_{\text{Caux\_ripple}}}. \tag{26}$$

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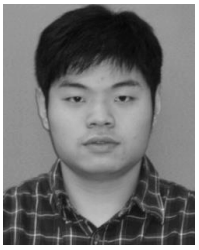

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