Topology and Control Innovation for Auxiliary Power Supply in Dimmable LED Drivers

Liang Jia, *Member, IEEE*, and Yan-Fei Liu, *Fellow, IEEE*

***Abstract*—In this paper, a cost-effective architecture based on Flyback topology is proposed for both constant current (CC) output for LED drive and constant voltage (CV) output for auxiliary (AUX) supply. A novel nonlinear ramp-based control scheme is proposed to decouple the main CC power train from the CV AUX supply and avoid LED output flickering. Small signal modeling is presented to highlight the advantages of this control scheme over conventional peak current mode control. This scheme has been implemented successfully for a 40-W dimmable LED driver with a 12-V 3-W AUX supply.**

***Index Terms*—Active cooling power supply, dimmable LED drivers, Flyback converter modeling, nonlinear ramp control, small-signal model.**

I. Introduction

DUE to the rapid transformation of lighting technology, light-emitting diode (LED) becomes the promising light source for the future world and provides: longer lifetime, higher energy efficiency, eco-friendly, better light quality, easier dimming, color control, etc., to the consumers. Unlike incandescent light source, LED requires a control gear (usually called LED driver) to provide a constant current (CC) driving current preferably for the best light output performance. As the Internet of Things (IoT) continues to proliferate, connected and smart solutions are influencing more and more areas of our lives, as well as lighting sector. From system point of view, the additional smart features will require separate power and voltage domains from LED load, therefore, integrating an auxiliary (AUX) power supply into LED drivers is an ideal option to facilitate LED luminaire system design and reduce system cost and complexity. This section comprises of a comprehensive overview of the latest trends for indoor dimmable LED drivers, including voltage window, 0–10-V dimming controls, and requirements for auxiliary power supplies.

A. Wide Operation Window and Dimming

One major challenge of designing LED driver (often being *ignored* in academic research) is the need of supporting a wide range of output voltage window [1]. The advantage of a wide voltage window driver is very obvious: 1) reduction of cost, number of stock keeping units and logistic complication; 2) reliability enhancement of LED load variation; and 3) system design flexibility, etc. An LED driver operation window can be defined using a V–I mapping [2]. In Fig. 1, two types of windows are illustrated, *A* type (red) and *B* type (blue) [3], [4]. In this example, the two types of operation windows have the same V_{LEDmin} and I_{LEDmin}. In both cases, the maximum LED voltage (V_{LEDmax}), minimum LED voltage (V_{LEDmin}), maximum LED current (I_{LEDmax}), and minimum LED current (I_{LEDmin}) are defined. In the LED lighting industry, for a high-performance LED driver, it often has a 2:1 window of V_{LEDmax}:V_{LEDmin} [3], [4]. The LED driver should provide protection for LED over voltage and over current and the levels are called V_{LEDOVP} and I_{LEDOCP}. Usually, the V_{LEDOVP} is 5–10% higher than V_{LEDmax} (only Type *B* V_{LEDOVP} is shown) and I_{LEDOCP} is defined based on the LED specifications. Also, driver may offer under voltage protection to prevent LED or driver damage during this abnormal condition and the V_{LEDUVP} level is usually 10% lower than the nominal V_{LEDmin}.

In both windows, the LED practical operating window is drawn in solid-line boxes. The slope of $\frac{\Delta V_F}{\Delta I_F}$ in the LED practical operating window is determined by the LED dynamic resistance [6]–[9]. In type *A* window, it is worth noticing that due to the LED dynamic resistance, a portion of the driver operation window cannot be practically used (for example, the red $*$ operating point in the window). For a reliable design, the driver should be able to operate properly and meet all the design specifications at the corner of $V_{\mathrm{LEDmax}} * I_{\mathrm{LEDmax}}$, i. e., $P_{\max}$. In order to extent the window for the same power capability, type *B* is introduced for alternative. The constant power line is defined for a power of $V_{\mathrm{LED}} * I_{\mathrm{LED}} = P_{\max}$. In this way both the V_{LEDmax} (B) and I_{LEDmax} (B) can be extended from the *A* type window. And the practical LED load operation window is, thus, extended significantly. *B* type window utilizes the power capability of the LED driver more efficiently.

Dimming control becomes very common for LED lighting application due to the simplicity of controlling light output by driving current [10]–[12]. A commonly used low-voltage dimming interface for indoor lighting is 0–10-V dimming interface. There are many different names of this interface, for example, Mark 7 dimming (first introduced by Philips in North America), 1–10-V dimming (in Europe), etc. And it was first introduced for dimmable fluorescent lighting system and adapted later into HID- and LED-based lighting (both indoor and outdoor

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L. Jia is with Consumer Hardware Engineering, Google Inc., Mountain View, CA 94043 USA (e-mail: jialiangleo@gmail.com).

Y.-F. Liu is with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3Y4, Canada (e-mail: yanfei.liu@queensu.ca).

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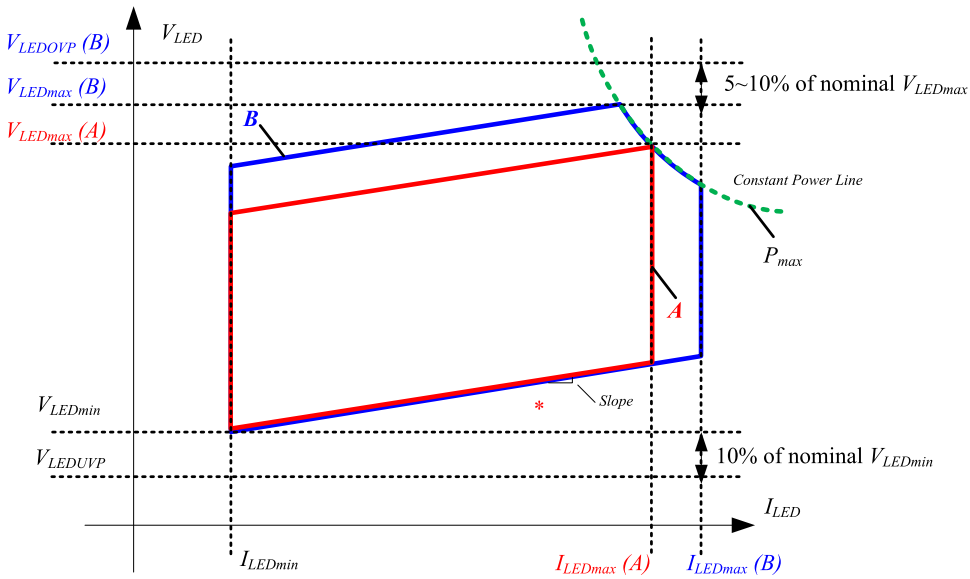

Fig. 1. LED driver operation window: A and B types.

TABLE I
HEAT AND ENERGY DISTRIBUTION OF VARIOUS WHITE LIGHT SOURCES

	White HBLED	Fluorescent	HID(Metal Halide)	60 W Incandescent
Visible Light	25–40%	21%	27%	8%
Infrared	~0%	37%	17%	73%
UV	0%	~0%	19%	0%
Total Radiant Energy	25–40%	58%	63%	81%
Remaining Heat	**60–75%**	**42%**	**37%**	**19%**

applications). The 0–10-V dimmer can be simply designed as a variable resistor and the ballast/driver has to provide a power source to generate a voltage potential between the two dimming leads (usually violet as positive, and gray as negative).

To sum up, for industrial LED applications, the LED driver has to support a wide range of LED load voltage and current, especially in dimmable applications.

B. Auxiliary Power Supply

Even though high-brightness LEDs (HBLEDs) are rapidly advancing in terms of energy efficiency, heat remains the nemesis of most HBLED illumination systems as shown in Table I generated by nonradiated recombination of electrons and holes in the HBLED semiconductor material. Although LEDs have the advantage of producing light in a narrow, well-defined wavelength, this also limits the devices' ability to radiate excess heat in the form of infrared energy [13], [14]; therefore, still around 60–75% of the LED power remains as heat [2], [15].

Other than increasing the heat sinking capacity in the LED luminaire, a growing number of indoor LED lighting applications will require forced-air convection because of the high intensity of light needed such as recessed light, spot light, and track light. Regular fans, however, introduce life time and reliability concern, and for indoor application the undesirable motor noise is also a disadvantage. A novel cooling solution is called SynJet cooler [14], [16]. These small coolers use an electromagnetically coupled diaphragm to pulse high-velocity jets of air through nozzles. As the air is forced out of the nozzle, a vortex is created. Once the vortex flow propagates downstream from the nozzle, it entrains the surrounding air [16]. The cooler requires 12-V dc power supply to provide dc + ac current.

Also, due to the downward-trending prices and limited price competition opportunities in "conventional" LED lighting, the ability to provide new value-added features, such as connectivity, enables additional growth potentials. Therefore, a deeper transition toward smart solutions becomes a natural direction for the entire LED lighting industry [5]. The idea that lighting can now communicate (via wireless network) and interact with the environment (via various sensors) and the people or things around it is opening up a new requirement for power delivery in the system to supply the added features. 12-V dc is a general voltage level to support multiple digital and analog voltage domains (5, 3.3 V, etc.) just like in computing application.

So from system point of view, a preferred low-medium power indoor LED driver architecture should offer a built-in auxiliary power supply for cooling or digital control/communication devices. A lot of research has been conducted for a single-stage Flyback LED driver with PFC for low-power application, however, the high output ripple at low frequency is not favorable for high-performance dimmable indoor application [17]–[23]. In [24]–[27], several methods have been discussed to reduce or cancel the low-frequency ripple. Boost PFC + Flyback topology is a low cost and good candidate for low-medium power LED application (25 W $< P_{\rm out} <$ 50 W). But it is very challenging to create a sufficient constant voltage (CV) auxiliary supply ($P_{\rm aux} >$ 2 W) directly from conventional Flyback topology for dimmable LED lighting application.

So, in this paper, a novel power architecture and control scheme is proposed to offer a decoupled CV power supply for the purposes of active cooling, lighting control, sensing, etc.,

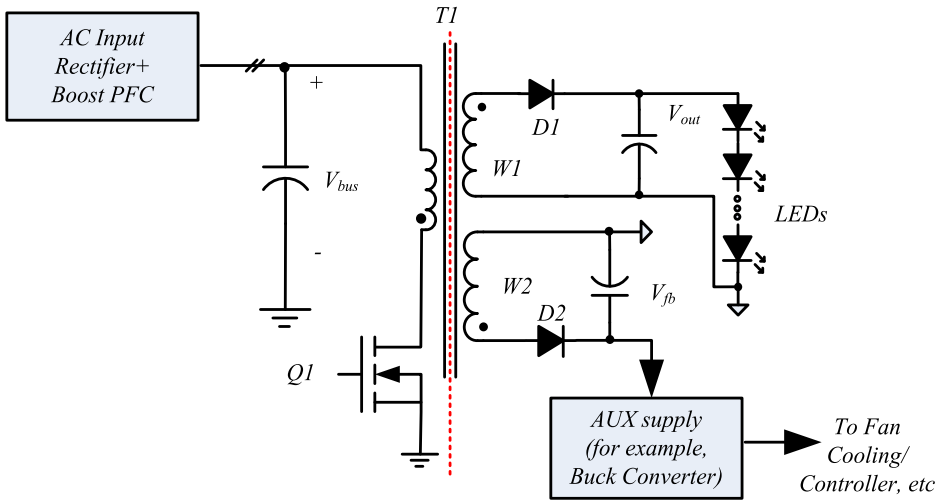

Fig. 2. AUX supply from a flyback winding.

from the same power converter, which outputs CC to the LEDs. In Section II, existing techniques and issues are introduced for research background. In Section III, the control scheme is outlined and the proposed scheme generates a nonlinear ramp to decouple the CV output from CC output and prevents from light flickering during fan operations in LED dimming condition. In Section IV, the operation and implementation of the proposed control scheme is explained in details. The implementation of the controller can be based on commonly used peak current mode (PCM) controller and no additional silicon development is required. In Section V, small signal model is built to analyze the advantages of the propose controller. Experimental results verify the benefits of this proposed LED driver architecture and control scheme in a 40-W 700-mA 0–10-V dimmable LED driver in Section VI. Finally, conclusion is drawn in the end of the paper. Appendix is also provided for detailed derivation for some of the critical design equations in the paper.

A version of this paper was presented at the ECCE 2014 conference [1]. The paper has been extended and improved, and derivation of critical design equations has been added.

II. Existing Techniques and Issues

In order to better illustrate the significance of the proposed technology, a detailed review of the existing techniques to create CV auxiliary supply is provided in this section.

There is a possibility of using auxiliary winding in the Boost PFC inductor to create an auxiliary power supply, however, 1) with peak detector output (diode rectifier and output capacitor) from either a flyback or forward winding, the rectified ac line voltage will be reflected to the auxiliary output, resulting in large voltage variation; and 2) with charge pump supply, the variation may also occur at line voltage zero crossing moment, due to higher current draw to support the constant auxiliary power. And overdesigned charge pump supply will require output voltage clamp to prevent from over voltage event at no load and very light load condition at the auxiliary output, resulting in unnecessary power losses. More importantly, in both cases, the commonly used PCM-controlled Boost PFC performance will be degraded, especially at line voltage zero crossing, when higher auxiliary current is reflected and added on top of the sensed Boost inductor current. Therefore, in this paper, the input ac rectifier and Boost PFC stage is ignored for simplicity and the input to the Flyback converter will be a well-regulated dc bus voltage.

The first solution is shown in Fig. 2, and a multioutput Flyback converter is used to generate the auxiliary supply. The flyback voltage $V_{\rm fb}$ is roughly proportional to the output voltage $V_{\rm out}$. However, as outlined in Section I, for a wide window LED driver (for example, $V_{\rm LEDmax} : V_{\rm LEDmin} = 3 : 1$), the variation of flyback voltage $V_{\rm fb}$ (the input of the auxiliary power supply) is 3:1 roughly. If nonideal transformer coupling is considered for different LED driving current scenarios, the voltage variation from the flyback winding will be much larger. Therefore, flyback winding is not suitable to provide a constant input level $V_{\rm fb}$ for the AUX supply. Otherwise, it requires a Buck–Boost stage to deal with the wide input range of $V_{\rm fb}$. For example, if the designer selects $V_{\rm fbmin} >$ 12 V at minimum number of LEDs to design the 12-V AUX supply using Buck converter, then at maximum number of LEDs, the $V_{\rm fbmax}$ will be larger than 36 V, efficiency will be compromised, and power component cost will be increased to handle higher voltage stress.

The second method is shown in Fig. 3. An additional Buck converter stage is powered directly from the LED main output. Other than the aforementioned range of $V_{\rm out}$ for AUX supply input, the operation of AUX supply will interrupt the main power train, resulting in LED output flickering or other light quality degradations. Expensive switcher *IC*/bulky configuration will be required for designing the Buck stage with $>$ 60-Vmax input.

The third method as shown in Fig. 4 is to use a separate Flyback converter powered from the high voltage dc bus for CV AUX supply. This configuration is used in some design that requires isolated standby power supply. During the standby mode, the main power train MOSFET Q1 will be off all the time, as well as the PFC stage. The $V_{\rm bus}$ will be the rectified line voltage filtered by $V_{\rm bus}$ capacitor and FET Q2 is controlled to regulate

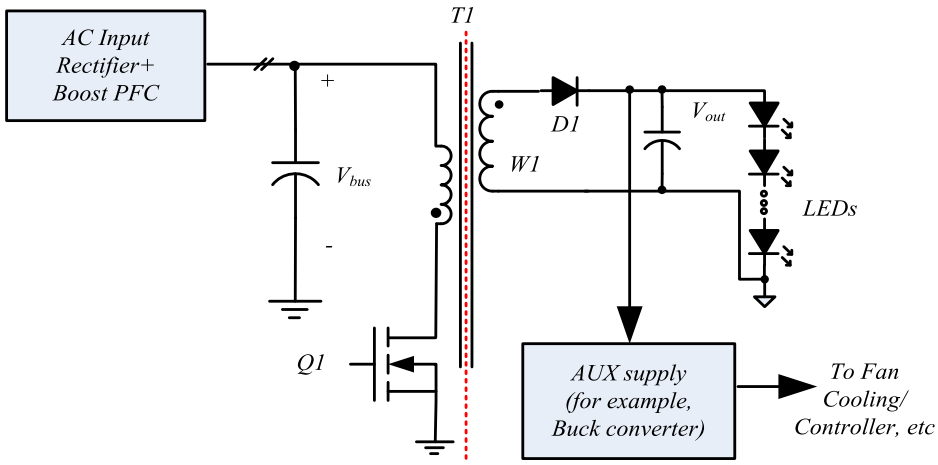

Fig. 3. AUX supply from main LED output.

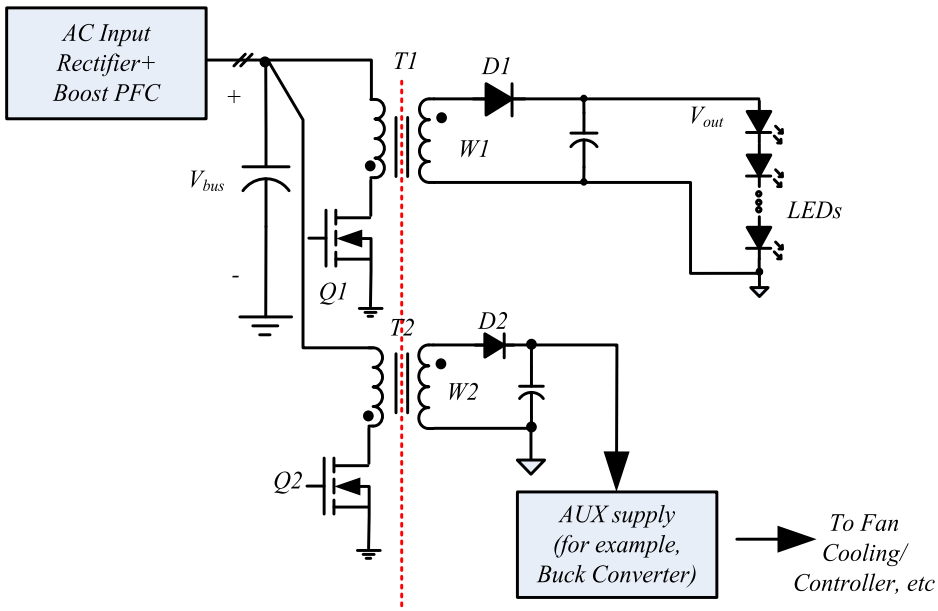

Fig. 4. AUX supply from a dedicated Flyback converter.

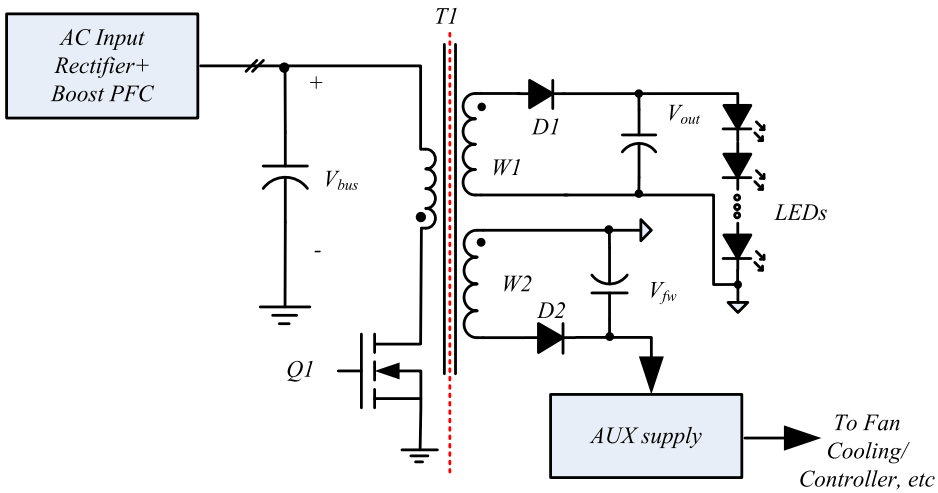

Fig. 5. AUX supply from a forward winding.

the AUX output voltage. However, in LED lighting application for thermal management purposes, the fan will only need to be operated when the LED light output power is high and additional heat dissipation is required. So for the auxiliary supply, the standby mode is not applicable. Although using this option, the AUX supply load is also completely independent from the main LED power train, the design will be bulky and more expensive because of the extra high voltage switch/switcher IC [28], isolation transformer, etc.

Another option is shown in Fig. 5, where a forward winding is used to provide a relatively constant dc voltage V_{fw} (about 20 V) from the dc bus and a Buck converter to step down this dc voltage for 12-V AUX supply. A cost-effective and commonly available switcher IC can be used for this AUX supply [31]. However, using conventional peak current mode control (PCMC), when the LED string is dimmed by dimmer, the AUX load starts affecting the main power train more severely and causing visible flicker at the LED output. This issue will be analyzed in more details in the next section.

This section provides a detailed review of the existing technology for generating a CV auxiliary power supply, including flyback winding supply, main output converter, dedicated Flyback converter, and a forward winding supply. The issue of each of the methods is also outlined.

III. Proposed Decoupling Methods

To resolve the issues discussed in the previous section, a new control scheme is presented in this section to decouple the AUX supply from the main LED driving power train.

The forward winding offers a relatively constant output voltage with fixed ratio to the dc bus voltage. This makes forward winding a promising option for this CV AUX application with lower cost and system complexity. At 40-W power level, where conduction loss is not yet dominant, BCM Flyback offers such benefits as smaller size of the magnetics (lower inductance) [29], higher efficiency (lower switching loss on the main FET with nearly voltage valley switching and zero current switching; lower output rectifier reverse recovery loss), etc., compared with CCM mode or fixed frequency Flyback with conventional voltage mode duty cycle control. Also, loop compensation will be more complicated due to the relatively lower frequency RHP zero in CCM Flyback converter [30]. So in this paper, the conventional PCMC is selected and used for Flyback converter control as illustrated in Fig. 6. In the case shown in Fig. 6(A), Flyback stage is operating without the AUX supply in BCM. V_e signal is the output from the error amplifier (EA). And the main FET Q1 sensing signal is $I_{Q1} * R_{\text{sense}}$ and as soon as the (1) is satisfied, Q1 will be turned off. Q1 turns back on again when the magnetizing current of T1 goes to zero

$$V_e = I_{Q1} \cdot R_{\text{sense}}. \tag{1}$$

However, once the forward winding is employed for the CV AUX, it is noted that the current reflected from forward winding I_{FW} will also be added to the main FET drain current I_{Q1} during t_{ON}. I_{FW} is varying with the AUX load demanding, V_{bus} low- frequency ripple, V_o, etc. The triangular shape of the sensing signal $I_{Q1} * R_{\text{sense}}$ is, thus, distorted. At full power or heavy LED load condition when $P_{\text{out}} >> P_{\text{aux}}$, flyback winding current I_{FB} is still dominant as shown in Fig. 6(B). But at LED dimming condition, the variant reflected forward winding current I_{FW} will start to dominate the $I_{Q1\text{peak}}$ shown in Fig. 6(C)

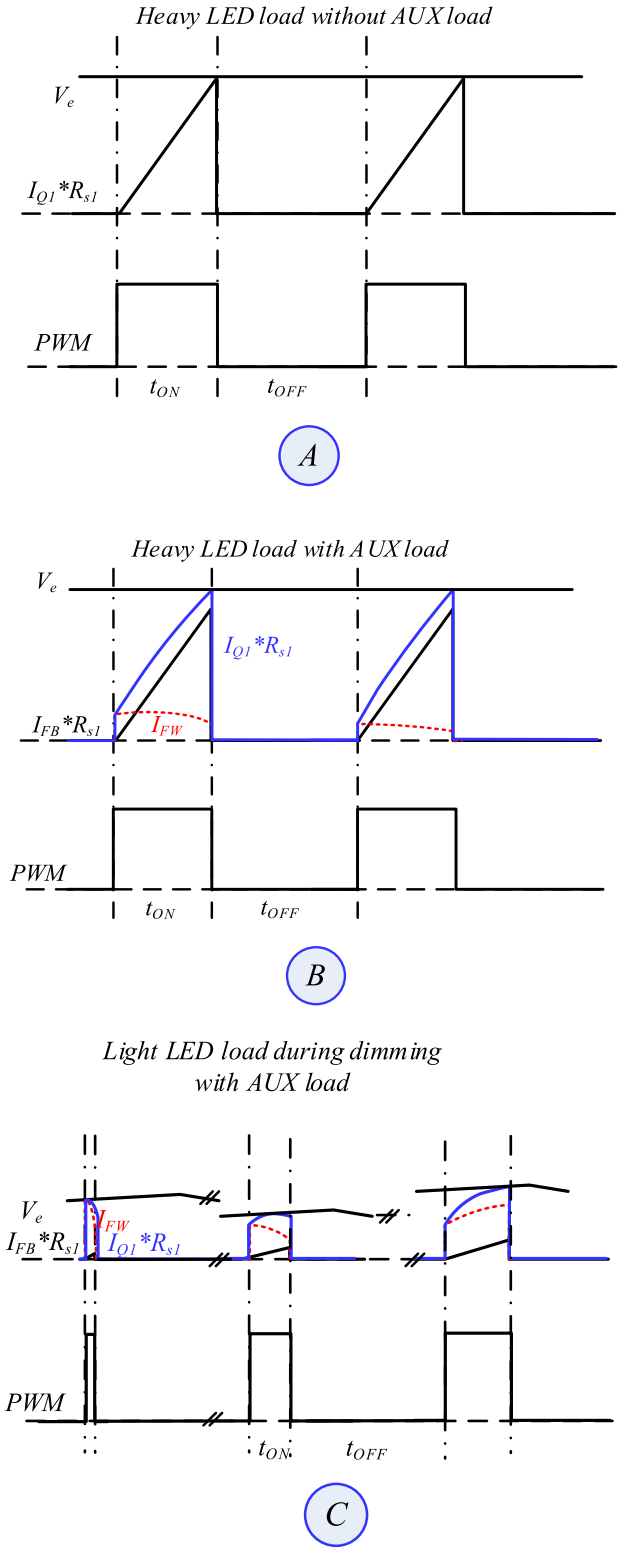

Fig. 6. Conventional PCMC.

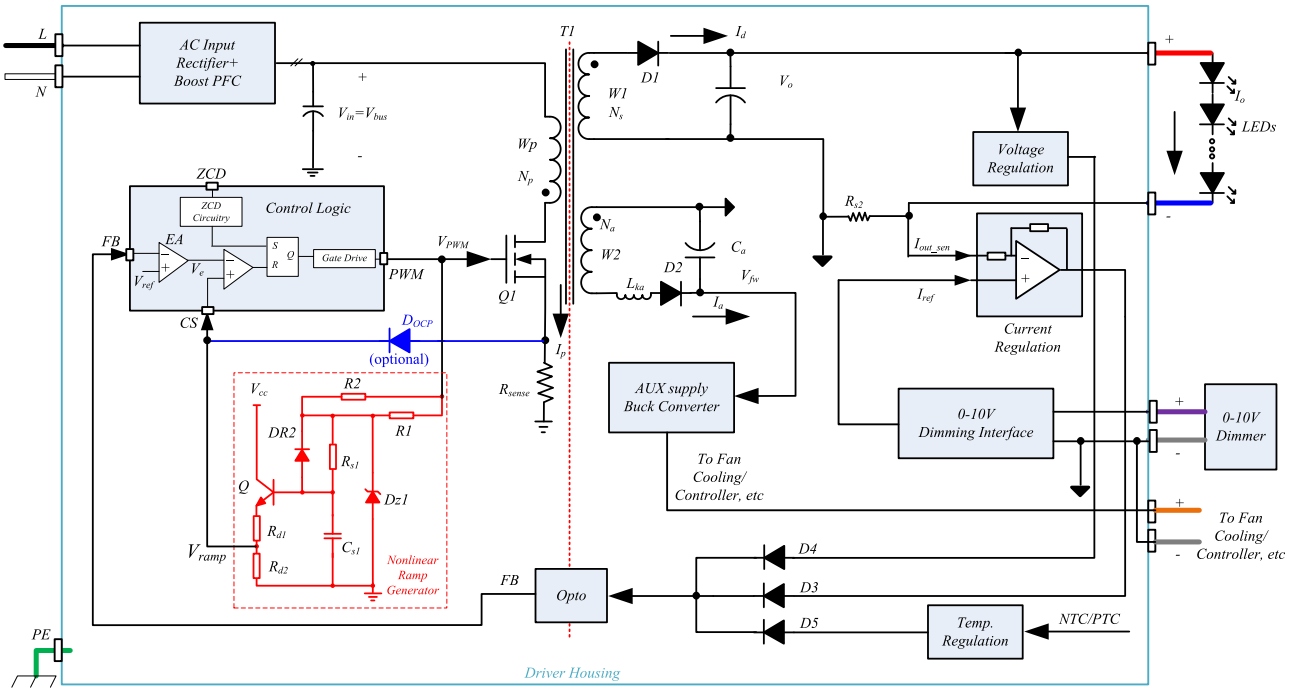

Fig. 7. Proposed system, functional blocks, and LED driver connection.

and the on time $t_{\rm ON}$ will vary a lot cycle by cycle, resulting in system instability and LED output random flickering.

Therefore, in order to take full advantage of the power architecture shown in Fig. 5, a novel control scheme is proposed to offer a decoupled CV auxiliary power supply for the purposes of active cooling, lighting control, sensing, etc., from the same power converter, which delivers CC to the LEDs. Proposed system and functional blocks are shown in Fig. 7. The 0–10-V dimmer is connected to the LED driver using the violet (positive) and gray (negative) wires and the dimmer circuit is shown in Fig. 23. The LED driver internal 0–10-V diming interface block will 1) provide bias current to the 0–10-V dimmer (150 μA, for example) and create a dc voltage (0–10 V in this case, according to the dimmer position) between violet and gray wires; and 2) read this dc voltage and translate it into $I_{\rm ref}$ for setting the output current reference in the current regulation loop. Different from the linear ramp signal from the sensed I_{Q1}, the control scheme generates a nonlinear ramp (highlighted in red in Fig. 7) to 1) decouple the CV output from CC output and prevents from light flickering during fan or other auxiliary load operations; 2) improve noise immunity of the controller at dimming condition; 3) reduce the variation of the system loop response at different operating conditions for easier compensation design; and 4) offer optional redundant over current and over power protection (OPP). The ramp signal $V_{\rm ramp}$ is generated (from the pulse width modulation (PWM) gate signal of the main FET Q1) to substitute the current sensing signal $I_{Q1} * R_{\rm sense}$ in the control scheme, as shown in Fig. 8(A)–(C). This $V_{\rm ramp}$ signal will then compare with V_e to turn off the FET in each switching cycle. The function of $V_{\rm ramp}$ is predefined to modulate $t_{\rm ON}$ based only on LED output regulation feedback loop (i.e., V_e signal), so $V_{\rm ramp}$ is not influenced by I_{FW} anymore. Detailed design guidelines will be provided in the next sections.

For example, in Fig. 7, when higher LED output current is desired, the current reference signal $I_{\rm ref}$ will be increased on the secondary side. And the secondary side EA will compensate the LED output current. Through the closed feedback loop control, V_e will be increased to V'_e. $V'_{\rm ramp}$, thus, follows to reach V'_e and finally extends $t'_{\rm ON}$ for larger LED output current in Fig. 8(A) (in dashed green). In another case, when LED current is under steady state, if AUX load is increased, $t_{\rm ON}$ will not be changed because of the unchanged $I_{\rm ref}$ and V_e, but I'_{FW} will be higher during $t'_{\rm ON}$ to provide more power for AUX load in Fig. 8(B) (in dashed red).

Besides the coupling impact, the instability at full *dimming* condition can be also caused by the very low sensing signal ($I_{Q1} * R_{\rm sense}$) level (at around 10 mV using conventional current mode control scheme), which is very sensitive to board noise (caused by $\frac{dv}{dt}$ and $\frac{di}{dt}$). So a nonlinear type of ramp signal is proposed and shown in Fig. 9, which has higher slew rate at the beginning of the charging process and then slows down until it reaches the V_e level.

For a typical application at this power level, the FET turn-on time $t_{\rm ON}$ is usually around hundreds of nanoseconds ($t_{\rm ONmin}$) to several microseconds ($t_{\rm ONmax}$). A proper time constant of $\tau = R_{s1}\,C_{s1}$ is selected accordingly, where $t_{\rm ONmin} < \tau < t_{\rm ONmax}$. In this way, at the beginning of the charging process, the $V_{\rm ramp}$ signal rises faster to get at least about 200-mV signal at full *dimming* condition ($V_{\rm ramp2}$ in Fig. 9). Compared with 10-mV level with conventional PCMC, this is one order improvement for better noise immunity. Also, in the next section, it will be shown that the nonlinear ramp actually reduces the system gain at dimming condition. At heavy LED load condition, a higher

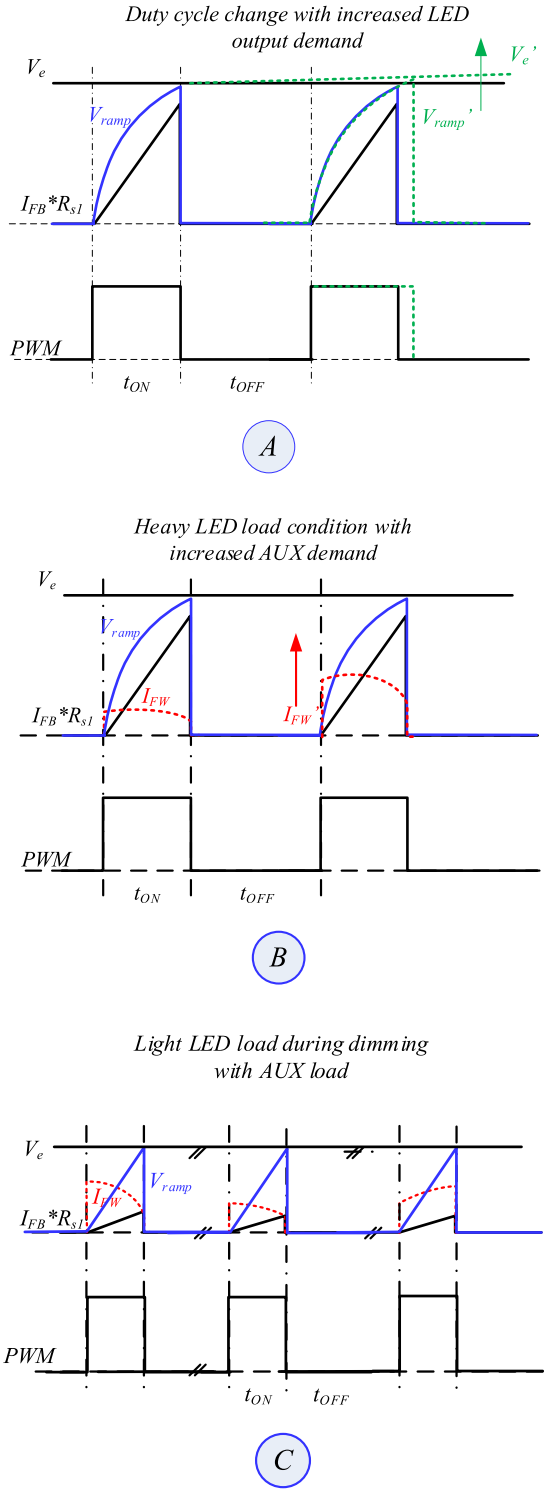

Fig. 8. Proposed nonlinear ramp control scheme.

$V_{\rm ramp}$ will be generated but $V_{\rm ramp}$ must be lower than over-current-protection (OCP) threshold to guarantee no OCP will be triggered in the Flyback stage. So, this scheme utilizes the saturated top of the nonlinear ramp in Fig. 8 to extend the output power capacity. This is the second benefit to use nonlinear ramp.

In many indoor LED lighting applications, where LED voltage is $<$ 60 V, the LED driver may be certified for UL Class 2 safety power units [32] and highly simplify the lighting fixture isolation design, resulting in lower system implementation cost as well. However, the UL Class 2 standard requires additional hardware and/or software redundancy in case of single-fault failure in the system to guarantee the safe output voltage and power. By adding a diode $D_{\rm OCP}$ to the existing current sense signal (see Fig. 7), there will be redundant OCP/OPP, in case of one implementation of the protection function is failed. For example, if the $R_{\rm sense}$ is shorted in a fault condition, the nonlinear ramp will still be able to fulfill the protection. During normal condition, the $D_{\rm OCP}$ will be reverse biased and will not impact the control scheme.

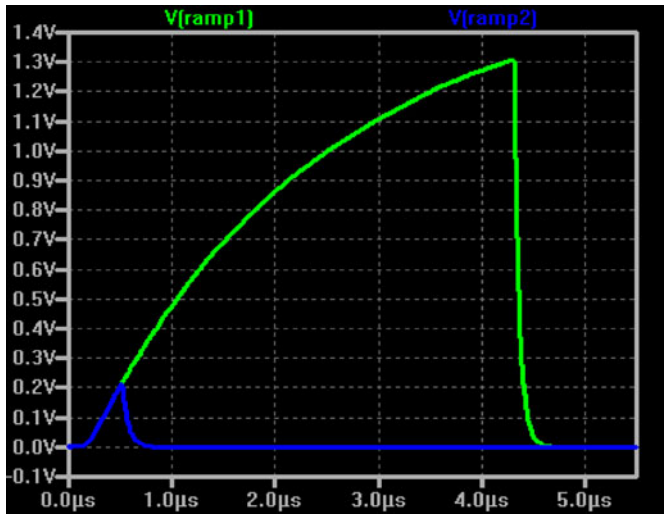

Fig. 9. Simulated nonlinear ramp signal (Green: ramp level at $t_{\rm ONmax}$; Blue: ramp level at $t_{\rm ONmin}$).

IV. Basic Operations and System Implementation

The system implementation diagram is shown previously in Fig. 7. The AUX supply is powered from forward winding W2 and D2. AUX supply block is typically a step down dc–dc switcher (for example, ST 5970D [31]) to create 12-Vdc, 250-mAmax supply. The input of the ramp generator is the gate signal from the gate control logic *IC*. The output of the ramp generator is called $V_{\rm ramp}$, which simulates the signal of $I_{Q1} * R_{\rm sense}$. The real current sensing signal ($= I_{Q1} * R_{\rm sense}$) is used for redundant OCP and OPP only. The gate control logic will compensate the loop according to the FB signal from secondary side (using built-in EA, the output of EA is called V_e) and turn off Q1 as soon as the $V_{\rm ramp} > V_e$. On the secondary side, the current regulation loop passes the feedback signal FB to the primary side across the isolation barrier through the optocoupler.

In Fig. 10, an analog circuit implementation of the ramp generator is shown. V_{PWM} is the gate signal from the gate control logic IC. R1 and Dz1 clamp the signal to a square waveform ($V_{\rm high} = V_{\rm gd}$). R_{S1} and C_{S1} form a *RC* time constant τ and the square waveform will be filtered to generate the ramp signal. When the gate signal V_{PWM} is at about 0 V, R2 and DR2 will help to quickly discharge C_{S1} to about 0.6 V. In order to compensate the diode forward voltage drop of DR2 and increase

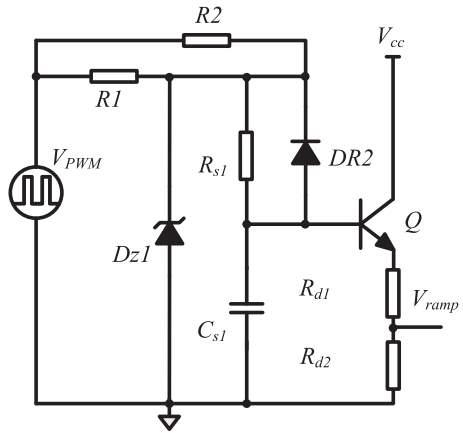

Fig. 10. Analog ramp generator.

loading capability, a bipolar emitter follower Q stage is used to condition the signal. Rd1 and Rd2 form a voltage divider for proper $V_{\rm ramp}$ signal level.

To properly design the nonlinear ramp generator circuit, the design rules are provided in (2)–(5). Based on the Flyback converter principles, the maximum turn-on time $t_{\rm ONmax}$ can be calculated using (2). Please refer to Appendix A for more details for derivation

$$t_{\rm ON\,max} = \frac{-\beta + \sqrt{\beta^2 - 4\alpha\gamma}}{2\alpha}. \tag{2}$$

And the parameter α, β, and γ can be calculated in (3)–(5). $V_{\rm inmin}$ is the minimum input dc voltage (425 V in this case) to the Flyback stage, in this case is the dc bus voltage. L_m is the primary magnetizing inductance of the transformer. C_{tot} is the total equivalent output capacitance of the MOSFET. $V_{o\max}$ is the maximum output voltage of the Flyback converter. $P_{o\max}$ is the maximum output power. V_F is the forward voltage of the output rectifier diode. η is the efficiency of Flyback power stage. Please refer to Appendix A for more details for derivation

$$\alpha = \frac{1}{2}\frac{{V_{\rm in\,min}}^2}{L_m} \tag{3}$$

$$\beta = -\frac{P_{o\,\max}}{\eta}\left(\frac{V_{\rm in\,min}}{n\left(V_{o\,\max}+V_F\right)}+1\right) \tag{4}$$

$$\gamma = -\frac{P_{o\,\max}}{\eta}\left(\pi\sqrt{L_m C_{tot}}\right). \tag{5}$$

Based on the calculation, the maximum $t_{\rm ON}$ at different operating points is shown in Fig. 11. At maximum power (700 mA and 60 V), $t_{\rm ON}$ is about 4.5 μs and at minimum power (70 mA and 20 V), $t_{\rm ON}$ is about 500 ns. And the results match the simulation closely shown in Fig. 9. In the experimental results section, it will demonstrate that the calculated results also match the experiments very well.

Finally, we need to make sure the voltage $V_{\rm ramp}$ in (6) to the gate control logic is less than the over current protection threshold level. In this way, we can tune the R_{S1} and C_{S1} to achieve maximum output power. In Fig. 12, the equivalent circuit of the ramp generator is shown. When the gate is off, the voltage of C_{s1} is clamped to the diode voltage V_{F_DR2} after the discharging of C_{s1} through *R2*. And the ramp voltage $V_{\rm ramp}$ at this moment will be roughly 0 V, due to the compensation between $V_{\rm be}$ of Q and V_{F_DR2}. When the gate drive voltage is high, the capacitor C_{s1} voltage will be charged up and the voltage of the ramp can be calculated in (6). $V_{\rm be}$ is the base-emitter voltage of Q and V_{F_DR2} is the forward voltage drop of DR2 in Fig. 10. $V_{\rm gd}$ is the clamping voltage of Dz1. It is noted that in (6), there are actually two design parameters: 1) the time constant $\tau = R_{s1}\,C_{s1}$ and 2) the divider ratio $\frac{R_{d2}}{R_{d1}+R_{d2}}$. So based on the desired peak ramp voltage levels for $t_{\rm onmin}$ and $t_{\rm onmax}$, the designer can solve these two parameters simply and flexibly

$$V_{\rm ramp} = \left[V_{F\_DR2} + V_{\rm gd}\left(1 - e^{\frac{-t_{\rm ON\,max}}{R_{s1}\cdot C_{s1}}}\right) - V_{\rm be}\right] \times \left(\frac{R_{d2}}{R_{d1}+R_{d2}}\right). \tag{6}$$

The relationship between control signal $V_{\rm ramp}$ and LED current I_o is plotted in Fig. 13. For example, when the LED load voltage is 60 V and current is 700 mA, the $V_{\rm ramp}$ peak value is about 1.3 V. While the LED load voltage is 20 V and current is 70 mA, the $V_{\rm ramp}$ peak level is around 200 mV. This result matches the simulation in Fig. 9 also very well.

V. Small-Signal Modeling

In this section, the small-signal model is derived to provide the insight of the coupling issue between CC and CV outputs using PCM control and the benefits of the proposed method.

Flyback converter can be analyzed with a Buck–Boost equivalent model shown in Fig. 14(left side). In the practical implementation, the leakage inductance of the Flyback transformer can be controlled lower than 1% of the magnetizing inductance, therefore, in the model, the leakage inductance is ignored. And the average large-signal model of a peak current controlled Flyback converter (in BCM) can be obtained by replacing the semiconductors Q1 and D1 in Fig. 14(left side) with dependent current sources $I_{\rm ac}$ and $I_{\rm pc}$ [33]–[40]. $I_{\rm ac}$ is the average current of the MOSFET Q1 and $I_{\rm pc}$ is the average current of the diode D1 over a switching cycle.

When the AUX supply is loaded and Q1 is on (see Fig. 7), the current flows through the diode D2 is near-constant and continuous due to winding leakage inductor L_{ka} and output filter capacitor C_a. It is assumed that the average AUX load current is I_a. The average output diode current I_d can be calculated in (7), where V_F is the forward voltage of D1, V_o is the output voltage, $V_{\rm in}$ is the bus voltage, $n = \frac{N_p}{N_s}$, and $n_a = \frac{N_p}{N_a}$. Please refer to Appendix B for more details for derivation of (7), using PCM control

$$I_d\left(V_{\rm in}, V_o, V_e, I_a\right) = \left(\frac{n\cdot V_e}{2R_{\rm sense}} - \frac{I_a\cdot\left[V_{\rm in}+n\left(V_o+V_F\right)\right]}{2n_a\cdot\left(V_o+V_F\right)}\right) \times \frac{V_{\rm in}}{V_{\rm in}+n\left(V_o+V_F\right)}. \tag{7}$$

The small-signal model can be obtained by setting all dc source values to zero (see Fig. 15). Then, I_d is linearized around

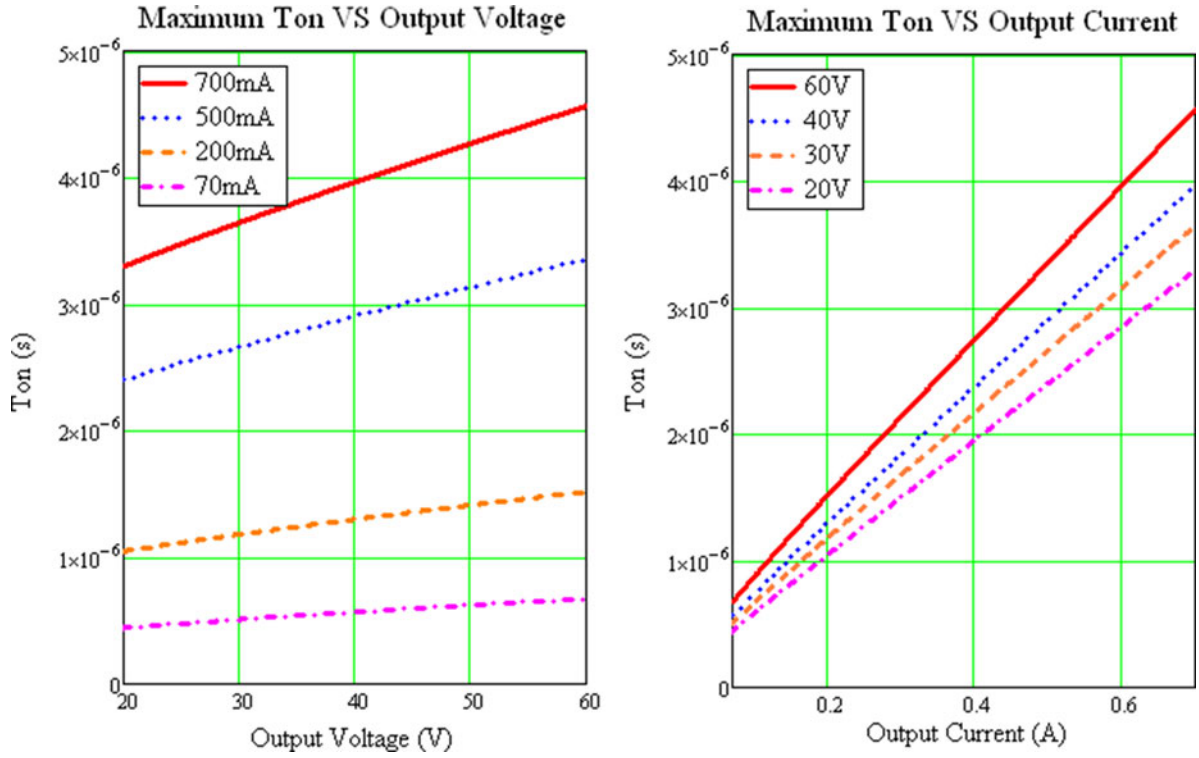

Fig. 11. Maximum t_{ON} time at different operating conditions at $V_{\mathrm{inmin}} = 425$ V.

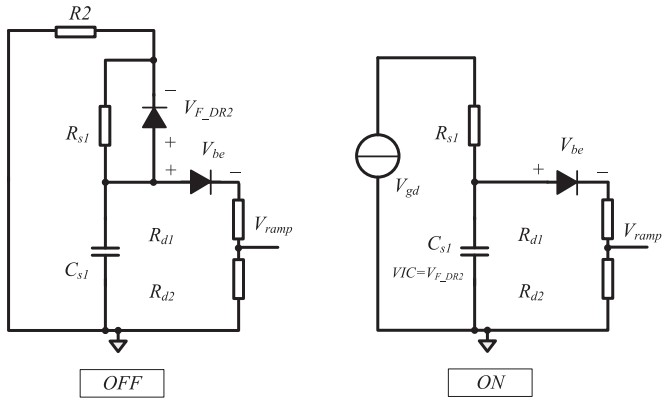

Fig. 12. Equivalent circuit for the ramp generator during ON and OFF modes.

its steady-state operating point in (2), where $K_e = \frac{\partial I_d}{\partial V_e}$, $K_{\mathrm{in}} = \frac{\partial I_d}{\partial V_{\mathrm{in}}}$, $K_o = \frac{\partial I_d}{\partial V_o}$, and $K_a = \frac{\partial I_d}{\partial I_a}$. The equations of K_e, K_{in}, and K_o for a Flyback converter without AUX load (i.e., $I_a = 0$) are presented in (9)–(11). It is noticed that in the small-signal model in (8), there is a coupling gain -K_a path from $\widehat{I_a}$ to $\widehat{I_d}$, where K_a can be calculated in (12), resulting in LED output flickering, while auxiliary loading is varying

$$\hat{I}_d = K_e \hat{V}_e + K_{\mathrm{in}} \hat{V}_{\mathrm{in}} + K_o \hat{V}_o - K_a \hat{I}_a \tag{8}$$

$$K_e = \frac{nV_{\mathrm{in}}}{V_{\mathrm{in}} + n(V_o + V_F)} \frac{1}{2R_{\mathrm{sense}}} \tag{9}$$

$$K_{\mathrm{in}} = \frac{nV_e}{2R_{\mathrm{sense}}} \frac{n(V_o + V_F)}{[V_{\mathrm{in}} + n(V_o + V_F)]^2} \tag{10}$$

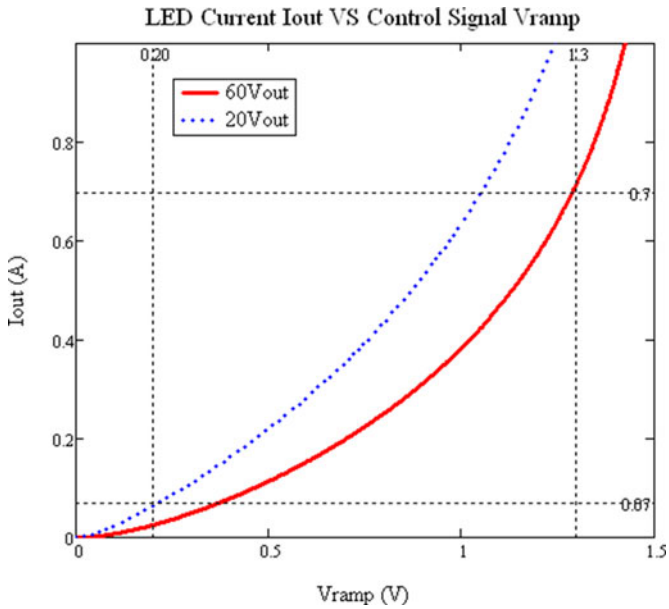

Fig. 13. LED current I_o versus control signal V_{ramp} at $V_{\mathrm{inmin}} = 425$ V.

$$K_o = -\frac{n^2 V_e}{2R_{\mathrm{sense}}} \frac{V_{\mathrm{in}}}{[V_{\mathrm{in}} + n(V_o + V_F)]^2} \tag{11}$$

$$K_a = \frac{V_{\mathrm{in}}}{2 \times n_a (V_o + V_F)}. \tag{12}$$

The transfer function from error voltage $\widehat{V_e}$ to output current $\widehat{I_o}$ is obtained in (13), where Z is the output impedance in (14)

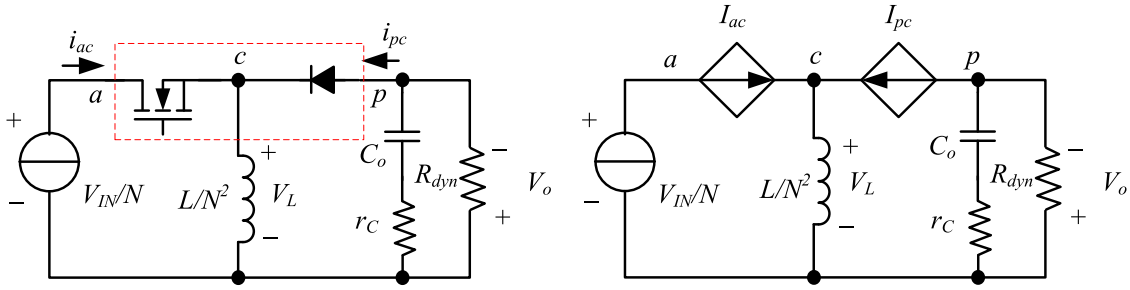

Fig. 14. Equivalent Buck–Boost Model for Flyback converter and average large signal model.

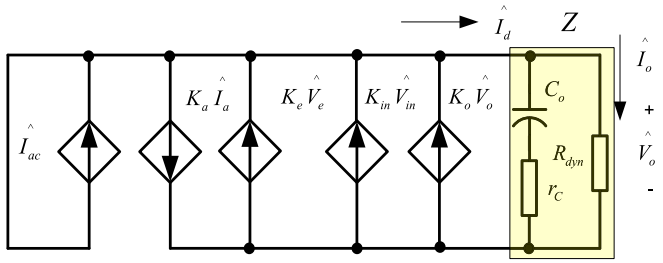

Fig. 15. Small signal model.

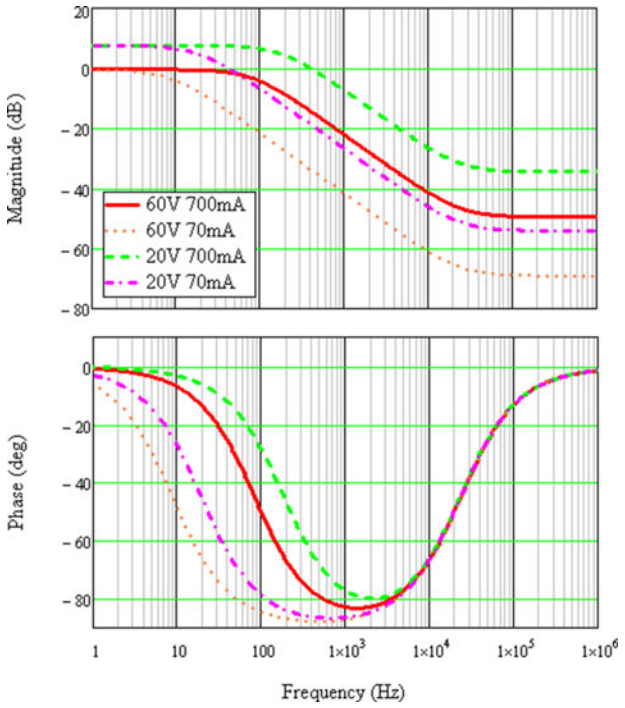

Fig. 16. Bode plot of $G_{\rm ie}$ for conventional PCMC.

and $R_{\rm dyn}$ is the LED dynamic resistance [8]

$$G_{\rm ie} = \left.\frac{\hat{I}_o}{\hat{V}_e}\right|_{\hat{V}_{\rm in}=0} = \frac{Z \times K_e}{R_{\rm dyn} \times (1 - Z \times K_o)} \tag{13}$$

$$Z = \frac{R_{\rm dyn}\,(1 + s \times C_o \times r_C)}{1 + s \times C_o \times (r_C + R_{\rm dyn})}. \tag{14}$$

Bode plot of $G_{\rm ie}$ for conventional PMC is shown in Fig. 16. When the Flyback stage is operating at $V_{\rm LEDmin} = 20$ V, the dc gain is higher and zero location is at higher frequency, compared with $V_{\rm LEDmax} = 60$ V (see Fig. 16) for the same output current. This explains that using the same compensator, Flyback LED driver stage is less stable when powering less number of LEDs.

Using the same modeling principles, the average diode current I_d of Flyback stage controlled by the proposed nonlinear ramp control scheme can be calculated as (15), where $t_{\rm ON}$ can be obtained in (16). Please refer to Appendix C for more details for derivation

$$I_d\,(V_{\rm in}, V_o, V_e) = \frac{n{V_{\rm in}}^2}{2L_m \times \left[V_{\rm in} + n\,(V_o + V_F) + \frac{TR \times n(V_o+V_F)}{t_{\rm ON}}\right]} \times t_{\rm ON} \tag{15}$$

$$t_{\rm ON} = -R_{s1}C_{s1} \ln\left(1 - \frac{V_e}{V_{\rm gd}} \frac{R_{d1}+R_{d2}}{R_{d2}}\right). \tag{16}$$

The small-signal model can be derived using (17), where ${K_e}' = \frac{\partial I_d}{\partial V_e}$, ${K_{\rm in}}' = \frac{\partial I_d}{\partial V_{\rm in}}$, and ${K_o}' = \frac{\partial I_d}{\partial V_o}$. The equations of K_e', $K_{\rm in}'$, and K_o' are represented as follows:

$$\hat{I}_d = {K_e}'\hat{V}_e + {K_{\rm in}}'\hat{V}_{\rm in} + {K_o}'\hat{V}_o \tag{17}$$

$${K_e}' = \frac{\partial I_d}{\partial V_e} = \left(\frac{\frac{n{V_{\rm in}}^2}{2L_m \times \left[V_{\rm in}+n(V_o+V_F)+\frac{{\rm TR}\times n(V_o+V_F)}{t_{\rm ON}}\right]}}{+\frac{n^2{V_{\rm in}}^2(V_o+V_F)\times {\rm TR}}{2L_m \times \left[V_{\rm in}+n(V_o+V_F)+\frac{{\rm TR}\times n(V_o+V_F)}{t_{\rm ON}}\right]^2 \times t_{\rm ON}}}\right) \times \left(\frac{R_{s1}C_{s1}\frac{R_{d1}+R_{d2}}{V_{\rm gd}R_{d2}}}{1 - \frac{V_e}{V_{\rm gd}}\frac{R_{d1}+R_{d2}}{R_{d2}}}\right) \tag{18}$$

$${K_o}' = \frac{\partial I_d}{\partial V_o} = \frac{-n^2{V_{\rm in}}^2\left(1 + \frac{\rm TR}{t_{\rm ON}}\right)}{2L_m\left[V_{\rm in} + n\,(V_o+V_F) + \frac{{\rm TR}\times n(V_o+V_F)}{t_{\rm ON}}\right]^2} t_{\rm ON} \tag{19}$$

$${K_{\rm in}}' = \frac{\partial I_d}{\partial V_{\rm in}} = \frac{n{V_{\rm in}}^2 + 2n^2V_{\rm in}V_o + \frac{2n^2V_{\rm in}V_o \times TR}{t_{\rm ON}}}{2L_m\left[V_{\rm in} + n\,(V_o+V_F) + \frac{{\rm TR}\times n(V_o+V_F)}{t_{\rm ON}}\right]^2} t_{\rm ON}. \tag{20}$$

It shows that the current $\widehat{I_d}$ is not related to $\widehat{I_a}$, but a function of $\widehat{V_o}$, $\widehat{V_{\rm in}}$, and $\widehat{V_e}$ in (17). So the output current is completely

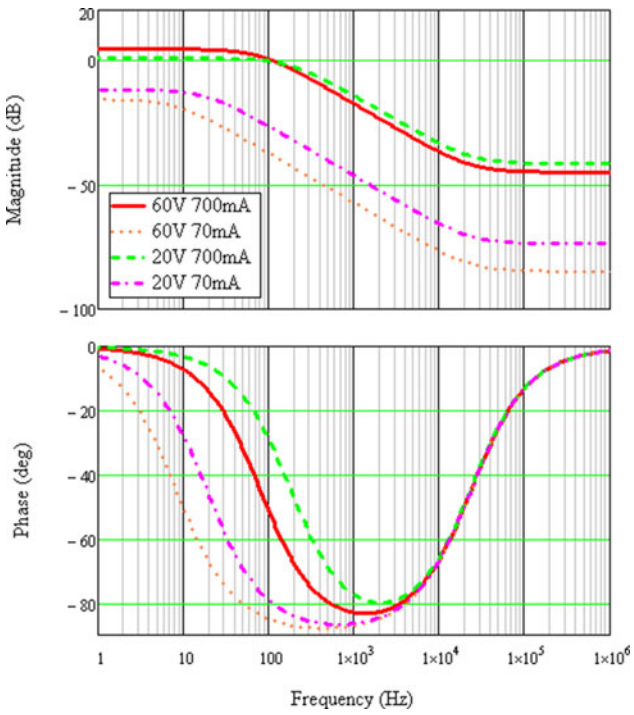

Fig. 17. Bode plot of $G_{\rm ie}$ for the proposed control scheme.

decoupled from the auxiliary load and also has the capability against V_o and $V_{\rm in}$ transients.

Similarly, the transfer function from error voltage $\widehat{V_e}$ to output current $\widehat{I_o}$ is obtained in

$$G_{\rm ie} = \left.\frac{\hat{I}_o}{\hat{V}_e}\right|_{\hat{V}_{\rm in}=0} = \frac{Z \times K_e{}'}{R_{\rm dyn} \times (1 - Z \times K_o{}')}. \qquad (21)$$

It is noticed that by using the proposed control scheme, when the Flyback stage is operating at $V_{\rm LEDmin} = 20$ V, the dc gain is reduced and getting closer to the case of $V_{\rm LEDmax} = 60$ V (see Fig. 17). At minimum current condition, the dc gain is also reduced to make the system easier to control for system stability.

VI. Experimental Verification

The design parameters of the prototype used in the experiments are shown in Table II.

In Fig. 18, at full output power, the $V_{\rm ramp}$ signal peak shown in CH2 (green) is close to 1.3 V and the maximum $t_{\rm ON}$ is about 4.5 μs and the maximum power 40 W can be achieved. This is very similar to the simulation in Fig. 9 and calculated results in Figs. 11 and 13. Compared with the real current sensing signal in CH3 (pink), $V_{\rm ramp}$ clearly shows a saturated nonlinear top. In the experiment, a fan load (1.8-W output power) is used as a worst case load with dc + ac current demand. The fan's vibrator is working during the higher half of the cycle, resulting in noisy current waveform in Fig. 18 CH1 (yellow).

In Fig. 19, LED output power $P_{\rm out} = 1.4$ W (3.5% of $P_{\rm max}$), the $V_{\rm ramp}$ signal peak is close to 200 mV and the minimum $t_{\rm ON}$ is about 500 ns. This is very similar to the simulation in Fig. 9 and calculated results in Figs. 11 and 13. The minimum power can be reached with the same fan load running at the same time.

TABLE II
Design Parameters in the Experimental Prototype

Design Parameter	Design Value or Description
$V_{\rm in}$	425 Vdc (min)
$V_{o\min}$	20 Vdc
$V_{o\max}$	60 Vdc
$I_{o\min}$	70 mA
$I_{o\max}$	700 mA
L_m	3.0 mHEE 25/16/9 core
L_k	Leakage inductance, 25 μH (max)
N	122:30
n_a	122:6
Q1	STF5N95K3, FET N 950 V 3.5 Ω TO-220FP
D1	2x ES2G in parallel, Diode, 400 V, 2A, SMB
R_{s1}	5.1 kΩ
C_{s1}	470 pF
R_{d1}	10 kΩ
R_{d2}	1.5 kΩ
$R_{\rm sense}$	2.7 Ω//2.7 Ω
LED Load	LUMILEDS LUXEON Rebel ES
Auxiliary Load	1.8-W Fan Load + 1.2-W Resistive Load

Fig. 18. Experimental results at full load (CH1-Yellow: fan current; CH2-Green: $V_{\rm ramp}$; CH3-Pink: I_{Q1}; CH4-Blue: V_{ds} of Q1).

From the zoom-in figure on the bottom, a stable switching is observed; even the FET current sensing signal (CH3: pink) is distorted by the fan load.

A MOSFET is used to switch the auxiliary load on and off with gate control signal in the following auxiliary load transient tests. The load consists of a resistive load and a cooling fan load. The additional resistive load is to increase the loading transient step and the slew rate, due to the slow ramping up of the fan load.

In Fig. 20, AUX load transient test is conducted at 0.1-Hz switching. The CH1 (yellow) signal is the load control switch voltage (drain to source), so during loading on the auxiliary supply, the switch is closed and zero voltage is across drain to source. While during the unloading step, the switch is OFF and about 12 Vdc is across the drain to source. From the zoom-in figure, it demonstrates a flat and noninterrupted output current in CH2 (green) at 20-V minimum LED voltage and 70-mA driving current (10% dimming).

Fig. 19. Experimental results at light load (CH1-Yellow: fan current; CH2-Green: V_{ramp}; CH3-Pink: I_{Q1}; CH4-Blue: V_{ds} of Q1).

Fig. 20. Transient performance during AUX load changes at 0.1 Hz (CH1-Yellow: control switch voltage of the auxiliary load, CH2-Green: load current at 70 mA, CH3-Pink: auxiliary load current, 1.2-W resistive load + 1.8-W fan load).

Fig. 21. Transient performance during AUX load changes at 1 kHz (CH1-Yellow: control switch voltage of the auxiliary load, CH2-Green: load current at 70 mA, CH3-Pink: auxiliary load current, 1.2-W resistive load + 1.8-W fan load).

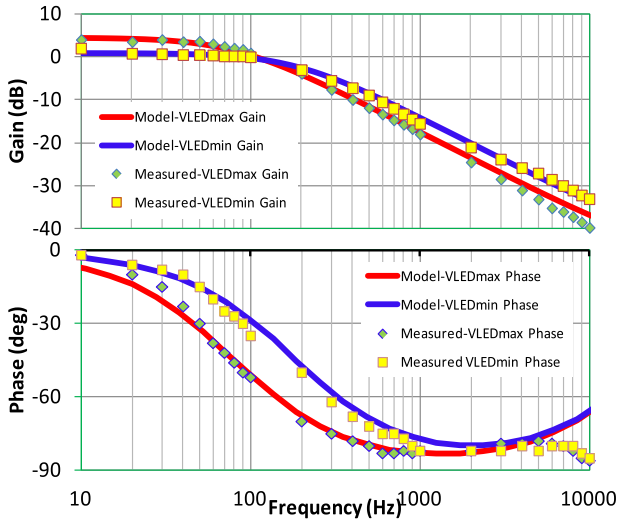

Fig. 22. Bode plot of G_{ie} for the proposed control scheme, mathematical model versus measurements.

In Fig. 21, 1-kHz AUX load transient test is conducted and in this case, the fan load is inactive. The CH1 (yellow) signal is again the load control switch voltage (drain to source), so during loading step, the switch is closed and zero voltage is across drain to source. While during the unloading step, the switch is off and about 12 Vdc is across the drain to source. From the zoom-in figure, it demonstrates a flat and noninterrupted output current in CH2 (green) at 20-V minimum LED voltage and 70-mA driving current (10% dimming).

The comparative Bode plots of G_{ie} are shown in Fig. 22 for the proposed scheme using mathematical model and experimental measurements. It demonstrates that the presented small-signal model is very accurate up to several kilohertz, where the system crossover frequency will locate. And beyond 10 kHz, the small-signal model based on the average value of each switching cycle starts to deviate from the measurement [45]. The system can be designed to be less sensitive for V_o change and the system dc gain is reduced at lower V_o ($V_{\mathrm{LEDmax}} = 60$ V, $I_{\mathrm{LEDmax}} = 700$ mA, $V_{\mathrm{LEDmin}} = 20$ V, $I_{\mathrm{LEDmin}} = 70$ mA).

A typical 0–10-V dimmer circuit is shown in Fig. 23. VR_{mk7}, $R_{\mathrm{mk7}}2$, C_{mk7} and Q_{mk7} form an adjustable voltage source. The voltage between base and emitter, V_{be} is used in this case as the reference voltage at about 0.6 V and the voltage between violet and grey leads can be calculated in (22). Z_{mk7} is for overvoltage protection when the user misconnects the dimmer to high voltages, such as ac mains

$$V_{\mathrm{dim}} \approx \frac{V_{\mathrm{be\_Qmk7}}}{R_{\mathrm{mk7}}2} \cdot (VR_{\mathrm{mk7}} + R_{\mathrm{mk7}}2)\,. \tag{22}$$

The ballast/driver will read the voltage different between violet and gray leads V_{dim} and control the light output. In Fig. 24, the dimming curves are measured with the prototype at different case temperatures of −20 °C, 25 °C, and 70 °C and AUX fan loading. A standardized 0–10-V dimming controller is used in the experiment and the driver outputs 100% when the diming voltage is larger than 8 V and 10% when the dimming voltage is lower than 1 V [3]. It demonstrates that the proposed topology and control scheme provide very stable and accurate output

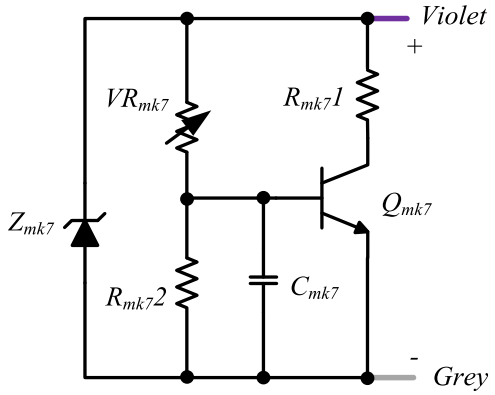

Fig. 23. A Simple 0–10 V/Mark 7 dimmer.

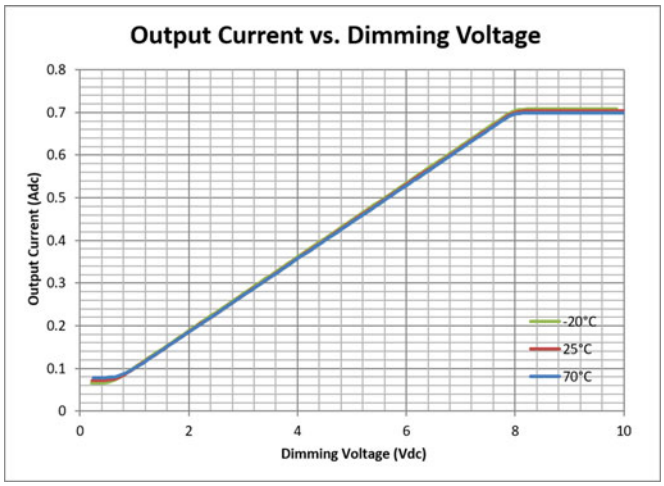

Fig. 24. Experimental dimming performance with AUX loading at different operating temperatures.

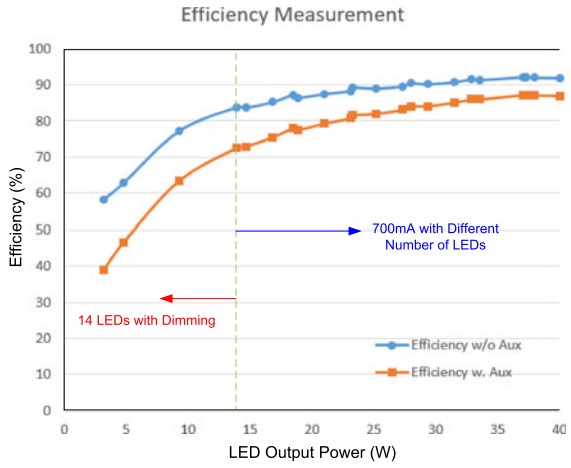

Fig. 25. Measured efficiency output LED load power versus the overall input power with and without auxiliary loading (with 1.8-W fan load).

driving current with wide dimming range and temperature variations.

The measured efficiency of the Flyback stage with and without auxiliary loading is shown in Fig. 25. 1.8-W fan is used for the loading during efficiency measurement. For more than 15-W output LED load power, the driver output current is 700 mA with different number of LEDs. And for below 15-W output power, the driver efficiency is measured with output current dimming. Without the auxiliary loading, the peak efficiency of the LED driver is approximately 92.1%, and with the 1.8-W auxiliary loading, the peak LED power efficiency is about 4.9% lower at approximately 87.2%. It is worth noting that the 1.8-W auxiliary loading (real power to the fan) is not included in the LED output power in the plot. So the efficiency drop, especially at low LED load power, is mainly due to this reason, and the actual total loss in the LED driver is not that much.

VII. Conclusion

In this paper, a novel control scheme is introduced to regulate CC LED output and CV AUX output at the same time for a Flyback-based LED driver architecture. Using a nonlinear ramp signal, the main CC output is decoupled from the CV auxiliary output, so that LED flickering issue at dimming condition is completely resolved. Advantages of the proposed method are explained by building the small-signal model. Based on the provided design guidelines, simulations and experimental results are presented to verify the proposed control scheme. Finally, experiments under steady state and auxiliary load transient confirm the effectiveness of the control scheme in the 40-W dimmable LED driver with a 12-V 3-W AUX supply.

Appendix

The derivation of critical equations in this paper will be shown in more details in this section.

A. Derivation of $t_{\rm ON}$ in (2)

Equation (2) is derived from the power delivery from the inductance L_m in the Flyback converter, where I_{pk} is the peak current of L_m and f_{sw} is the switching frequency

$$P_{\rm in} = \frac{P_o}{\eta} = \frac{1}{2} \times L_m {I_{pk}}^2 f_{\rm sw} = \frac{1}{2} \times L_m \left(\frac{V_{\rm in}}{L_m} \times t_{\rm ON} \right)^2 \times \frac{1}{t_{\rm ON} + t_{\rm dis} + {\rm TR}} \tag{23}$$

where $t_{\rm dis}$ is the discharging time of the magnetizing current, which can be calculated in (24). And TR is the quasi-resonant duration, which can be found in (25):

$$t_{\rm dis} = \frac{V_{\rm in}}{n\left(V_o + V_F\right)} t_{\rm ON} \tag{24}$$

$${\rm TR} = \pi \sqrt{L_m C_{\rm tot}}. \tag{25}$$

Substitute (24) and (25) into (23), we can then obtain

$$\frac{1}{2} \times \frac{{V_{\rm in}}^2}{L_m} \times {t_{\rm ON}}^2 - \frac{P_o}{\eta} \left(\frac{V_{\rm in}}{n\left(V_o + V_F\right)} + 1 \right) \times t_{\rm ON} - \frac{P_o}{\eta} \left(\pi \sqrt{L_m C_{\rm tot}} \right) = 0. \tag{26}$$

And the $t_{\rm ON}$ can be solved using (2) finally and only the positive solution will be taken.

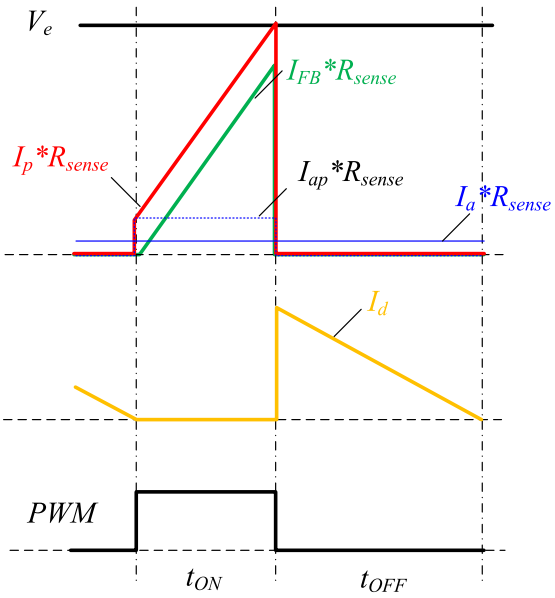

Fig. 26. Waveform for derivation of (7).

B. Derivation of I_d in (7)

First, the current of the auxiliary load I_a is reflected to primary side when the main FET turns on and the average value of this current $I_{\rm ap}$ during on time can be found in (27) and geometry of the waveform is shown in Fig. 26.

$$I_a = \frac{I_{\rm ap} \times t_{\rm ON} \times n_a}{t_{\rm ON} + t_{\rm OFF}} \Leftrightarrow I_{\rm ap} = \frac{I_a \left(t_{\rm ON} + t_{\rm OFF}\right)}{t_{\rm ON} \times n_a}. \quad (27)$$

To calculate the average current I_d, we can use (28) to obtain the peak of the $I_{\rm FB}$, $I_{\rm FB\_pk}$ in Fig. 26 and then reflect this value to secondary side and average it over the switching period in (29):

$$I_{\rm FB\_pk} = \frac{V_e}{R_{\rm sense}} - I_{\rm ap} = \frac{V_e}{R_{\rm sense}} - \frac{I_a \left(t_{\rm ON} + t_{\rm OFF}\right)}{t_{\rm ON} \times n_a} \quad (28)$$

$$I_d = \frac{I_{\rm FB\_pk} \times n \times t_{\rm OFF}}{2\left(t_{\rm ON} + t_{\rm OFF}\right)} = \frac{\left(\frac{V_e}{R_{\rm sense}} - I_{\rm ap}\right) \times n \times t_{\rm OFF}}{2\left(t_{\rm ON} + t_{\rm OFF}\right)}. \quad (29)$$

Finally, we can substitute (27) into (29) and in order to simplify the equation in an explicit form without losing the insight of the coupling between I_a and I_d, we assume in (29), $t_{\rm OFF} = t_{\rm dis}$. However, in Fig. 16, we still consider the time duration TR, which is the difference between $t_{\rm OFF}$ and $t_{\rm dis}$.

C. Derivation of I_d in (16)

Using the nonlinear ramp proposed in this paper, the $t_{\rm ON}$ can be derived from

$$V_e = V_{\rm gd}\left(1 - e^{-\frac{t_{\rm ON}}{R_{s1}C_{s1}}}\right)\frac{R_{d2}}{R_{d1} + R_{d2}}. \quad (30)$$

Similar to the derivation of (7), we can obtain the peak of the $I_{\rm FB}$, $I_{\rm FB\_pk}$ on the primary side and calculate the average value of I_d over a switching cycle on the secondary side as in

$$I_d = \frac{I_{\rm FB\_pk} \times n \times t_{\rm dis}}{2\left(t_{\rm ON} + t_{\rm OFF}\right)} = \frac{\left(\frac{V_{\rm in}}{L_m} \times t_{\rm ON}\right) \times n \times t_{\rm dis}}{2\left(t_{\rm ON} + t_{\rm dis} + TR\right)}. \quad (31)$$

Substitute (24) and (25) into (31), we can obtain (16).

ACKNOWLEDGMENT

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Liang Jia (S'08–M'12) received the B.Eng. degree from the School of Mechanical and Electrical Engineering, Soochow University, Suzhou, China, in 2008, and the Master's of Applied Science degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2011.

Since January 2015, he has been a Power Lead for Consumer Hardware and Power Architect for dc–dc (48 V-PoL) power technology for Global Datacenter Infrastructure at Google Inc., Mountain View, CA, USA. From 2011 to 2015, he was a Product Design Engineer with Philips Electronics North America, Rosemont, IL, USA. His main responsibility was to develop new-generation high-power LED drivers with digital intelligence and better performance. His current research interests include power management, power delivery for high performance and supercomputing, battery management, LED lighting systems, resonant power conversion, digital control technology, modeling and simulation, next-generation 48 V-PoL voltage regulators, power semiconductor devices, and integrated circuits.

Mr. Jia has published 20 technical papers in IEEE Transactions and conferences and three IP defensive publications and has 12 US and international patents pending. He received the National Scholarship of China in 2008, Temasek Foundations (Singapore)-Nanyang Technological University LEaRN Scholarship in 2008, Tsung-Dao Lee Chinese Undergraduate Research Endowment in 2006, and about ten other scholarships and awards during his studies. He served as a section Chair in IEEE ECCE 2015 and he is also a reviewer for the IEEE TRANSACTIONS ON POWER ELECTRONICS, *Industrial Electronics*, *Industry Applications*, and *Industrial Informatics*.

Yan-Fei Liu (M'94–SM'97–F'13) received the Bachelor's and Master's degrees from the Department of Electrical Engineering, Zhejiang University, Zhejiang, China, in 1984 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

He was a Technical Advisor with the Advanced Power System Division, Nortel Networks, Ottawa, ON, Canada, from 1994 to 1999. Since 1999, he has been with Queen's University, where he is currently a Professor with the Department of Electrical and Computer Engineering. His current research interests include digital control technologies for high efficiency, fast dynamic response dc–dc switching converter and ac—-dc converter with power factor correction, resonant converters, and server power supplies, and LED drivers. He has authored over 200 technical papers in the IEEE Transactions and conferences, and holds 20 US patents. He is also a Principal Contributor for two IEEE standards. He received Premier's Research Excellence Award in 2000 in Ontario, Canada. He also received the Award of Excellence in Technology in Nortel in 1997.

Dr. Liu serving as an Editor of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS OF POWER ELECTRONICS (IEEE JESTPE) since 2013, an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2001, and a Guest Editor-in-Chief for the special issue of Power Supply on Chip of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2011 to 2013. He also served as a Guest Editor for special issues of JESTPE: Miniaturization of Power Electronics Systems in 2014 and Green Power Supplies in 2016. He serves as a Co-General Chair of ECCE 2015 held in Montreal, QC, Canada, in September 2015. He will be the General Chair of ECCE 2019 to be held in Baltimore, MD, USA. He has been the Chair of PELS Technical Committee on Control and Modeling Core Technologies since 2013 and the Chair of PELS Technical Committee on Power Conversion Systems and Components from 2009 to 2012.