DC-Link Capacitor Voltage Balancing Technique for Phase-Shifted PWM-Based Seven-Switch Five-Level ANPC Inverter

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***Abstract*—The Five-Level Active-Neutral-Point-Clamped (5L-ANPC) inverters are receiving more attentions as one of preferred solutions for medium and high power applications because of the combination of the features of the conventional Flying-Capacitor (FC) type and Neutral-Point-Clamped (NPC) type inverters. This paper proposes a new DC-link capacitor voltages balancing technique for the Seven-Switch 5L-ANPC (7S-5L-ANPC) topology which is using Phase-Shifted PWM (PS-PWM) modulation method. Based on the power relationship between DC-link capacitors and FC, the proposed technique adjusts the duty cycles of redundant 1-level switching states to balance the DC voltage without changing the output performance. The proposed technique can be applied to any 5L-ANPC inverter topologies. A 1 kW single-phase 7S-5L-ANPC inverter experimental prototype is built to verify the effectiveness of the proposed DC-link capacitor voltages balancing technique.**

***Keywords*—Multilevel inverter; Active-Neutral-Point-Clamped (ANPC) inverter; Flying-Capacitor; Pulse-Width-Modulation (PWM)**

I. INTRODUCTION

Multi-level inverter is a preferred solution for medium and high power applications because of the lower voltage switch stress, lower Total Harmonic Distortion (THD), lower Electromagnetic Interference (EMI) and higher efficiency as compared with its two-level opponent [1]–[4]. There are three types of the conventional multi-level inverter topologies: the Neutral-Point-Clamped (NPC) type [5], the Flying-Capacitor (FC) type [6] and the Cascaded H-Bridge (CHB) type [7]. When the number of output levels increases, a large number of NPC diodes, FCs and isolated DC sources are required for NPC, FC and CHB multi-level inverters respectively. The complexity of balancing the voltages of DC-link capacitors for NPC and FC types and FC voltages for FC type is increased.

The hybrid multi-level inverters are receiving more attentions recently because they combine the features of many conventional multi-level inverter topologies [8], [9]. As one of the most popular hybrid multilevel inverter topologies, the Five-Level Active-Neutral-Point-Clamped (5L-ANPC) inverter combines the characteristics of NPC type and FC type inverters [10]–[14]. Compared to the conventional five-level NPC and FC types inverters, the 5L-ANPC inverter only employs two DC-link capacitors, one FC and eight active switches, so the system costs, volume and complexity of capacitor voltages balancing are reduced. In order to further decrease the number of active switches, a Seven-Switch 5L-ANPC (7S-5L-ANPC) is proposed recently [15], as shown in Fig. 1. The analysis shows the 7S-5L-ANPC inverter is capable of achieving the same performance as the conventional 5L-ANPC inverters for high power factor applications such as Photovoltaic (PV) grid-tied application (power factor > 0.9).

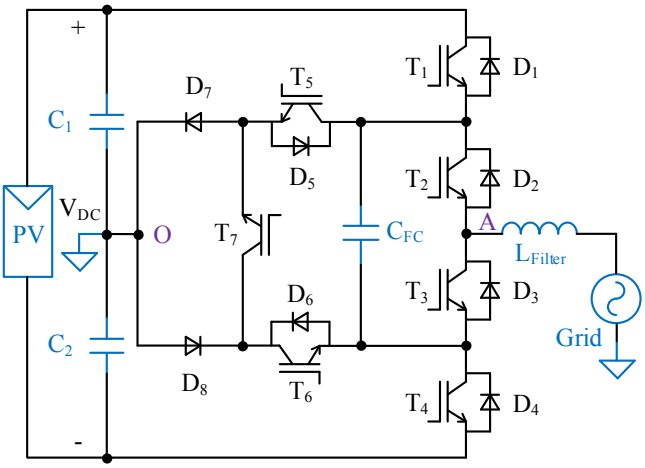

Fig. 1. Configuration of the 7S-5L-ANPC inverter.

The capacitor voltage balancing is an important issue for 5L-ANPC inverters. In [16]–[18], the Space Vector Modulation (SVM) is used to generate five-level output and balance the voltages of DC-link capacitors and FC. In [19], [20], the technique of zero sequence voltage injection is used to balance the DC-link capacitor voltages. However, these methods are only suitable for three-phase applications. For single-phase application, the carrier-based Pulse Width Modulation (PWM) is usually used to generate switching patterns. In [21]–[23], the Phase-Shifted PWM (PS-PWM) is used as modulation strategy. The advantage of using PS-PWM is the self-balancing of FC

voltage and low FC voltage ripple. However, how to balance the DC-link capacitor voltages using PS-PWM is not discussed. Reference [24] designed a DC-link capacitor voltage balancing technique based on Phase-Disposition PWM (PD-PWM) method for single-phase application.

In this paper, a new DC-link capacitor voltages balancing technique for 7S-5L-ANPC inverter with PS-PWM modulation is proposed. Based on the power relationship between DC-link capacitors and FC, the proposed technique adjusts the duty cycles of redundant 1-level switching states to balance the DC voltage without changing the output performance. This balancing method can be applied to any 5L-ANPC inverter topologies. The paper is organized as follows. In Section II, the operating principles and PS-PWM strategy of 7S-5L-ANPC inverter are introduced. Section III presents the proposed DC-link capacitor voltages balancing for 7S-5L-ANPC inverter using PS-PWM. Section IV and V give the simulation and experimental results and Section VI draws the conclusion.

II. Operating Principles of 7S-5L-ANPC Inverter

A. Configuration of the 7S-5L-ANPC Inverter

The configuration of the 7S-5L-ANPC inverter is shown in Fig. 1. The input DC voltage is defined as V_{DC}. The DC-link consists of two series-connected capacitors (C_1, C_2), whose voltages are rated at half of DC voltage ($V_{DC}/2$). A flying-capacitor (C_{FC}) is required to provide one quarter of DC voltage ($V_{DC}/4$). The five output level $+V_{DC}/2$, $+V_{DC}/4$, 0, $-V_{DC}/4$ and $-V_{DC}/2$ (which are defined as +2, +1, 0, -1 and -2 respectively for simplification) are obtained by summing algebraically the DC-link capacitors and FC voltages. Two discrete diodes D_7 and D_8 act as the body diode of switch T_7 to limit the reverse voltage, so the selection of T_7 can be IGBT without anti-parallel diode, reducing the system cost. In addition, the current through T_7 under unity power factor condition will be zero, and under high power factor condition a low current is passing through T_7. Therefore, for high power factor applications such as PV grid-connected system, a low current rating device can be selected for T_7, leading to a further system cost reduction.

B. Operating Principles of the 7S-5L-ANPC Inverter

Same as the conventional 5L-ANPC inverters, the 7S-5L-ANPC inverter has eight switching states to generate five output levels. The relationship between eight switching states (A to H), output voltage levels and their impact on FC voltage is given in Table I. The output current and FC voltage are defined as i_{out} and V_{FC} respectively.

From Table I it is observed that there are three pairs of redundant switching states generating the same output levels: +1 (B and C), 0 (D and E) and -1 (F and G). Additionally, four 1 level switching states (B, C, F and G) are capable of changing the FC voltage. Therefore, the FC voltage can be balanced by appropriate selection of 1 level redundant switching states.

C. PS-PWM strategy for 7S-5L-ANPC Inverter

The PS-PWM strategy has been used in Three-Level (3L) ANPC inverter [25] to achieve apparent switching frequency doubling, and it has also been applied to the conventional 5L-ANPC inverter due to the self-balancing of FC voltage and lower FC voltage ripple. This method can also be applied to the 7S-5L-ANPC inverter topology. Fig. 2 shows the diagram of PS-PWM for the 7S-5L-ANPC inverter. In this case, the reference signal V_{ref} can be written as:

$$V_{ref} = \begin{cases} M \cdot \sin(\omega t), & \sin(\omega t) \geq 0 \\ M \cdot \sin(\omega t) + 1, & \sin(\omega t) < 0 \end{cases} \quad (1)$$

where M is the modulation index ($0 \leq M \leq 1$) and ω is the phase angle frequency. V_{ref} is compared with two carrier waves S_{d1} and S_{d2} that are phase shifted on the horizontal axis by half switching period $T_S/2$. The switching patterns of seven active switches in one switching period T_S are analyzed in four different cases: (a) $0 < M \cdot \sin(\omega t) \leq 0.5$. (b) $0.5 < M \cdot \sin(\omega t) \leq 1$. (c) $-0.5 \leq M \cdot \sin(\omega t) < 0$. (d) $-1 \leq M \cdot \sin(\omega t) < -0.5$.

The gate signals of T_1, T_4 and T_7 are determined by V_{ref} and S_{d1}. During the positive grid cycle, T_1 is turned ON when $V_{ref} > S_{d1}$; T_1 is OFF for the whole negative grid cycle. Similarly, T_4 is switched ON when $V_{ref} < S_{d1}$ during negative grid cycle and is OFF for the whole positive grid cycle. When T_1 or T_4 is ON, T_7 must be switched OFF to prevent FC being connected directly to the DC-link capacitor.

Carrier signal S_{d2} determines the switching states of T_2 and T_3. When $V_{ref} > S_{d2}$, T_2 is ON and T_3 is OFF; when $V_{ref} < S_{d2}$, T_2 is OFF and T_3 is ON. Switches T_5 and T_6 are operated at line frequency based on the polarity of output current. As can be observed, switches T_1, T_2, T_3, T_4 and T_7 commute at switching frequency f_S, and the output voltage V_{AO} has an apparent switching frequency equal to $2f_S$. In addition, using PS-PWM method, the 1 level redundant switching states (B, C, F and G) will be applied alternately, leading to FC voltage self-balancing and reduced FC voltage ripple [26], [27].

TABLE I. Switching States, Output Voltage and Impact on the FC Voltage of 7S-5L-ANPC Inverter

Switching state	Conduction state of active switch							Output voltage level	Flying capacitor C_{fc}		Conduction state of T_7
	T_1	T_2	T_3	T_4	T_5	T_6	T_7		$i_{out} > 0$	$i_{out} < 0$	
A	1	1	0	0	0	1	0	+2	--	--	No
B	1	0	1	0	0	1	0	+1	Charge	Discharge	No
C	0	1	0	0	0	1	1	+1	Discharge	Charge	Yes
D	0	0	1	0	0	1	1	+0	--	--	Yes
E	0	1	0	0	1	0	1	-0	--	--	Yes
F	0	0	1	0	1	0	1	-1	Charge	Discharge	Yes
G	0	1	0	1	1	0	0	-1	Discharge	Charge	No
H	0	0	1	1	1	0	0	-2	--	--	No

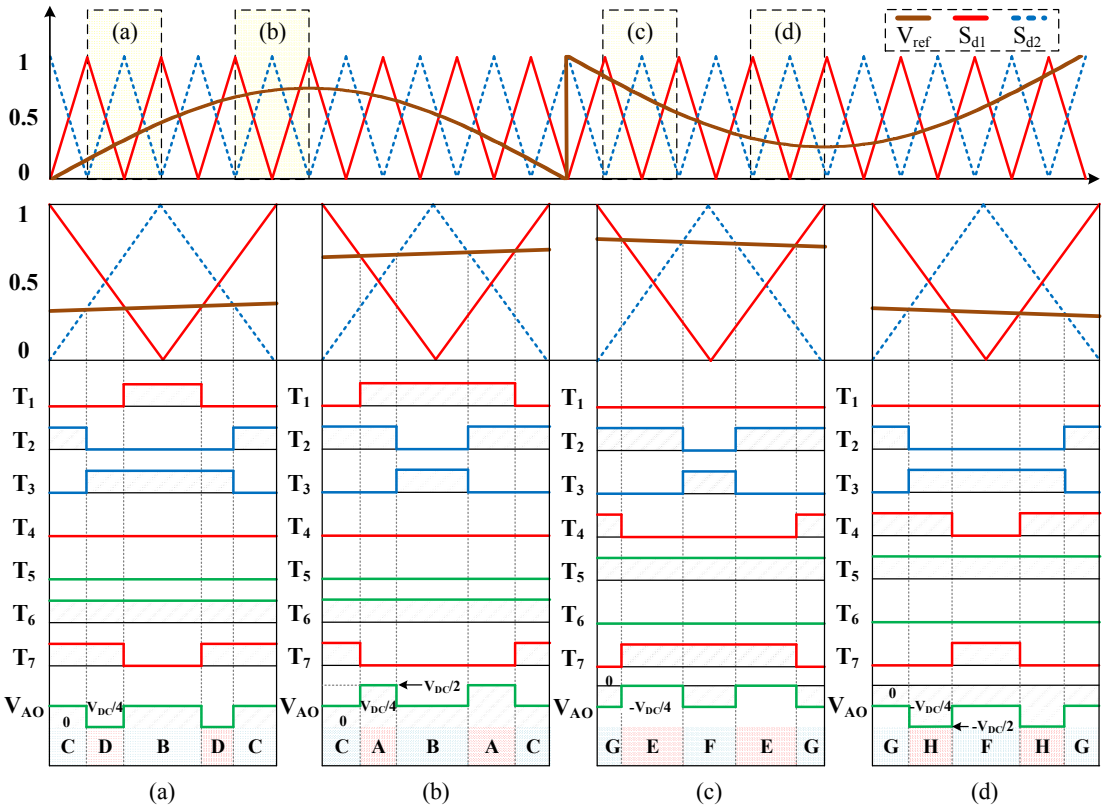

Fig. 2. PS-PWM for the 7S-5L-ANPC inverter. (a) $0 < M \cdot \sin(\omega t) \le 0.5$. (b) $0.5 < M \cdot \sin(\omega t) \le 1$. (c) $-0.5 \le M \cdot \sin(\omega t) < 0$. (d) $-1 \le M \cdot \sin(\omega t) < -0.5$.

III. DC-Link Capacitor Voltages Balancing Technique with PS-PWM

The DC-link capacitor voltages balancing is an important issue for 5L-ANPC topologies. Most previous DC balancing techniques are only suitable for three-phase application such as zero sequence voltage injection. In this section, a new DC-link capacitor voltage balancing technique for the 7S-5L-ANPC inverter with PS-PWM is proposed, which can be used for single-phase as well as three-phase applications.

A. Power Transmission Relationship Between FC and DC-link Capacitors

The 5L-ANPC inverters are half-bridge based inverter topologies. For single-phase 5L-ANPC inverters, the output power in positive grid cycle is provided by the upper DC-link capacitor C_1 and FC; similarly, the lower DC-link capacitor C_2 and FC are transferring the energy to the output side during negative grid cycle. If the inverter is controlled to generate symmetrical output current, then the power relationship can be obtained

$$\Delta P_{C1} + \Delta P_{FCP} = \Delta P_{C2} + \Delta P_{FCN} \tag{2}$$

where ΔP_{C1}, ΔP_{FCP} is the energy offered by C_1 and FC in positive grid cycle respectively; ΔP_{C2}, ΔP_{FCN} is the energy from C_2 and FC in negative grid cycle respectively. The power transmission relationship is depicted in Fig. 3.

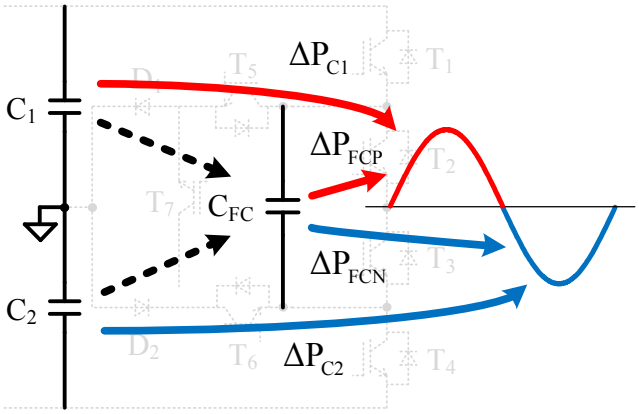

Fig. 3. Power transmission relationship between DC-link capacitors and FC for the 5L-ANPC inverters.

B. DC-Link Capacitor Voltages Balancing with PS-PWM

During 0 level freewheeling state, the output side is disconnected from DC-link capacitors and FC, so the voltages of DC capacitor and FC are unchanged. It is only possible to regulate the DC capacitor voltage during 1 and 2 level switching states. When inverter is required to generate +2 level output, only state A can be used, which means the transmitted power from state A is fixed; similarly, only state H can be used to generate -2 level, so the power from state H is also fixed.

Therefore, the redundant 1 level switching states (B, C) and (F, G) not only have impact on FC voltage regulation but also play an important role in controlling the DC capacitor voltages. Fig. 4 shows the circuit diagram of four 1 level switching states. The red solid line represents the active current path while the green dashed line shows the reactive current path. It is observed that the variation of DC-link capacitors and FC voltages depends on the polarity of output current. The impact of output current polarity on voltages of three capacitors during four 1 level switching states is listed in Table II. Signals + and – represent charging and discharging respectively. Take switching state B for example. When $i_{out} > 0$, the upper side DC capacitor C_1 is providing the energy to the output side and charging the FC, so C_1 is discharging. To maintain the input DC voltage V_{DC} constant, the voltage of lower side DC capacitor V_{C2} will be increased accordingly, achieved by the preceding DC-DC stage or input DC source.

As mentioned earlier, with PS-PWM, the redundant 1 level switching states are applied alternately, so the total operating time of redundant 1 level switching states is approximately the same. To regulate the DC-link capacitor voltages, the duty cycles of each 1 level switching state can be adjusted.

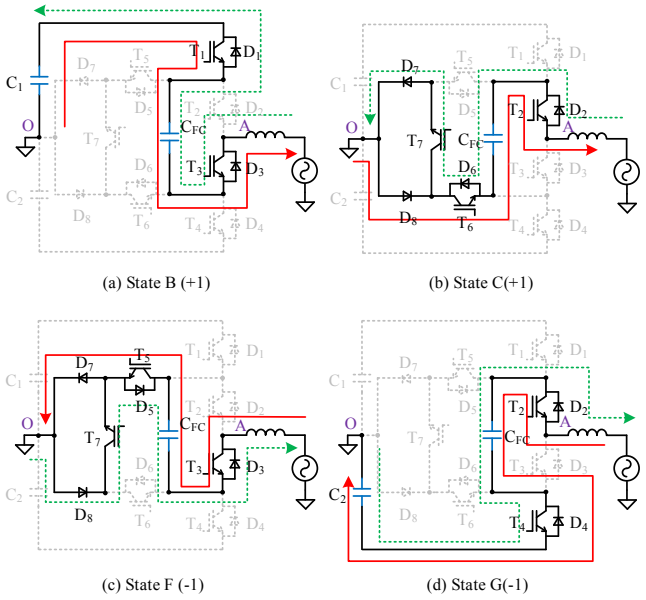

Fig. 4. Four 1 level switching states for 7S-5L-ANPC inverter.

TABLE II. IMPACT OF THE POLARITY OF OUTPUT CURRENT ON 1 LEVEL SWITCHING STATES ON DC-LINK CAPACITORS AND FC VOLTAGES

Switching State	Impact on V_{C1}		Impact on V_{C2}		Impact on V_{FC}	
	$i_{out} > 0$	$i_{out} < 0$	$i_{out} > 0$	$i_{out} < 0$	$i_{out} > 0$	$i_{out} < 0$
B (+1)	-	+	+	-	+	-
C (+1)	No change	No change	No change	No change	-	+
F (-1)	No change	No change	No change	No change	+	-
G (-1)	-	+	+	-	-	+

Take the unbalanced situation when V_{C1} is greater than V_{C2} for instance. During positive grid cycle, if $i_{out} > 0$, according to Table II, it is possible to increase the duty cycle of state B by Δd and also reduce the duty cycle of state C by Δd accordingly, then the output voltage will remain unchanged, but C_1 is discharging more; if $i_{out} < 0$, the duty cycle of state B is reduced by Δd, and the duty cycle of state C is increased by Δd to ensure the output voltage, so C_1 is charging less. Thus the voltage difference between two DC capacitors will be decreased. The duty cycle adjustment for states F and G is done in a similar way during negative grid cycle to decrease the DC capacitor voltage difference.

It should be noted that the variation of duty cycles of 1 level redundant switching states will also change the FC voltage, which means under transient state the FC voltage is not balanced in $V_{DC}/4$. But in steady state, the duty cycles of 1 level redundant states will be closed to each other so that FC voltage will be naturally balanced [19].

With above analysis, the control diagram of DC-link capacitor voltage balancing with PS-PWM is designed, as shown in Fig. 5. First, after the closed-loop control, the reference voltage signal V_{ref} is calculated, and then it is compared with two carrier signals S_{d1} and S_{d2} to generate the gate signals of each switch. The gate signals are sent to 1 level switching state duty cycle adjustment block for duty cycle correction.

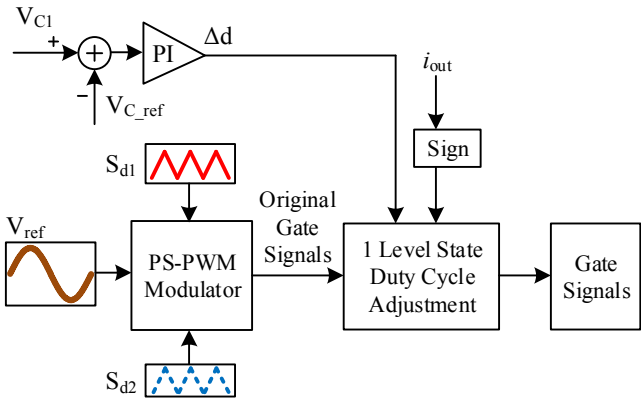

Fig. 5. Control diagram of DC-link capacitor voltage balancing using PS-PWM.

As mentioned earlier, to adjust the 1 level state duty cycle, the information of 1) DC-capacitor voltage and 2) polarity of output current is required. Therefore, one of DC-capacitor voltage (e.g. V_{C1}) needs to be sampled, which is then compared with the reference value V_{C_ref} which is half V_{DC}. The error is sent to PI controller to generate the duty cycle variation value Δd. With Δd, the polarity of output current i_{out} and information of switch gate signals, the duty cycles of 1 level redundant switching state can be adjusted.

Due to the symmetry, the implementation of 1 level switching state duty cycle adjustment is evaluated in two cases during positive grid cycle: (a) $0 < M \cdot \sin(\omega t) \le 0.5$; (b) $0.5 < M \cdot \sin(\omega t) \le 1$, as shown in Fig. 6. After analyzing the information of DC capacitor voltage and output current polarity, then whether the duty cycle of states B and C should be increased or

decreased is known. For example, if duty cycle of state B should be increased by Δd and state C is decreased by Δd, then the turn-on time of T_1 and T_3 is increased by Δt symmetrically and the turn-on time of T_2 and T_7 is decreased by Δt symmetrically:

$$\Delta t = \Delta d \cdot T_S \tag{3}$$

As can be observed, with the adjustment, the duty cycles of state D (0 level) and A (+2 level) are unchanged, but the duty cycles of states B and C are changed accordingly. After the 1 level switching state duty cycle adjustment, the updated gate signals of all seven switches are sent to gate driving circuits to trigger all seven switches. The proposed DC balancing technique can be applied to any 5L-ANPC topologies which use PS-PWM strategy.

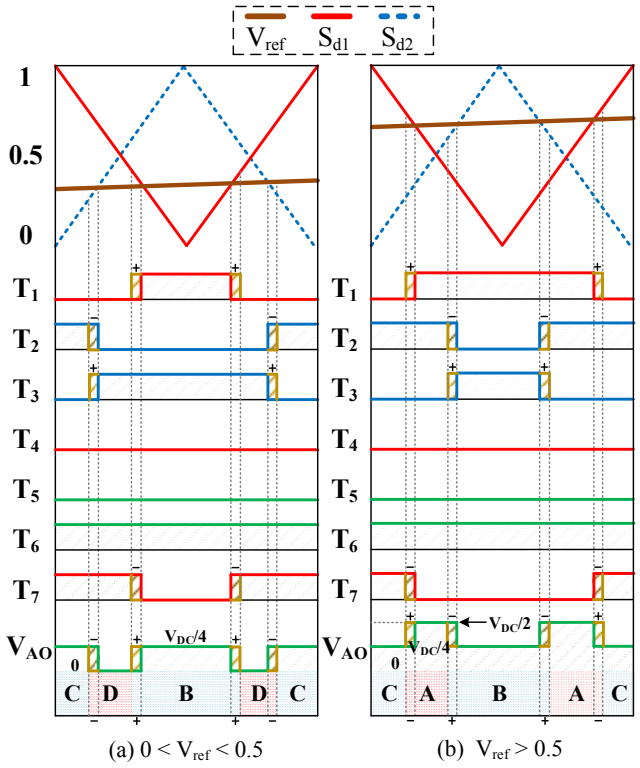

Fig. 6. 1 level switching state duty cycle adjustment with PS-PWM.

IV. Simulation Verification

To verify the effectiveness of proposed DC-link capacitor voltage balancing technique, the computer simulation by MATLAB/Simulink has been carried out to verify their effectiveness. The system parameters are shown in Table III.

TABLE III. System Parameters

Power	1 kW	**Grid Voltage (RMS)**	110 V @ 60 Hz
DC-link Voltage	400 V	**Output Filter Inductance**	2.6 mH
FC Capacitance	310 μF	**Carrier Frequency**	5 kHz
DC Capacitance	2000 μF each	**Output Current (RMS)**	9.1 A

To show the importance of DC-link capacitor voltages balancing for 5L-ANPC topologies, a comparison between the 7S-5L-ANPC inverter without and with the DC-link capacitor voltage balancing is made. The comparison results are shown in Fig. 7. The waveforms of output voltage V_{AO}, DC capacitor voltages V_{C1}, V_{C2} and FC voltage V_{FC} using PS-PWM without DC balancing are shown in Fig. 7 (a) and (b). It is observed that the system has DC-link voltage divergence problem if not controlled, the reason of which is analyzed in details in [24]. With the proposed method, the DC-link voltage divergence is solved, as shown in Fig. 7 (c) and (d). As can be observed, the voltage of each DC capacitor is balanced in 200 V.

Fig. 8 shows the simulation results of the 7S-5L-ANPC inverter using PS-PWM with the proposed DC balancing technique in steady state. Fig. 8 (a) shows the five-level bridge voltage. Fig. 8 (b) shows the two DC-link capacitor voltages and FC voltage. The measured line-frequency ripple of DC-link capacitor voltage is 14.3 V (= 14.3 V/200 V = 7.15 %), and the measure FC voltage ripple is 2.4 V (= 2.4 V/100 V = 2.4 %). Fig. 8 shows the grid voltage and output current. The output current is in phase with the grid voltage. The measure output current THD is 0.85 %, as shown in Fig. 8 (d).

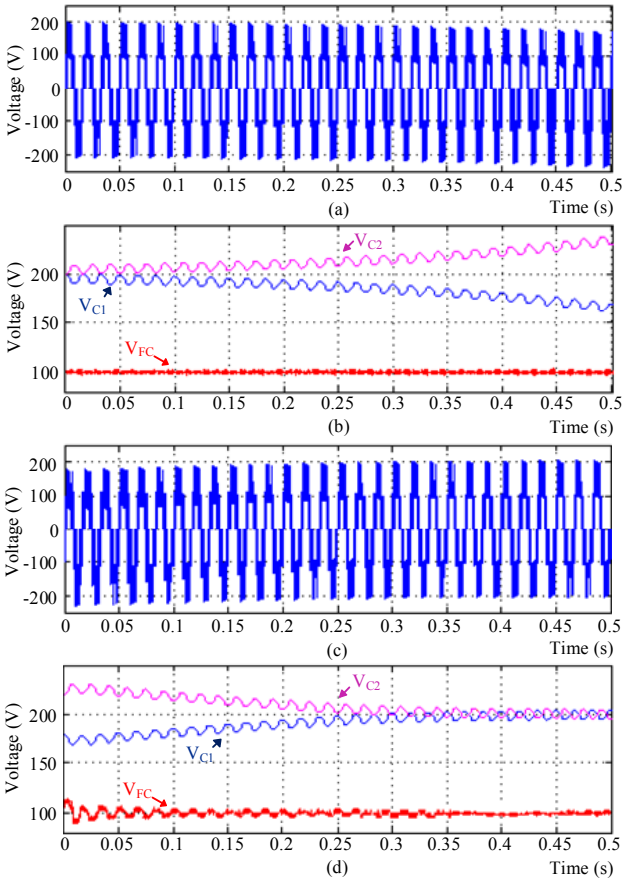

Fig. 7. Simulation results using PS-PWM without and with the proposed DC balancing technique. (a) Output voltage without DC balancing. (b) DC capacitor voltages and FC voltage without DC balancing. (c) Output voltage with the proposed DC balancing technique. (d) DC capacitor voltages and FC voltage with the proposed DC balancing technique.

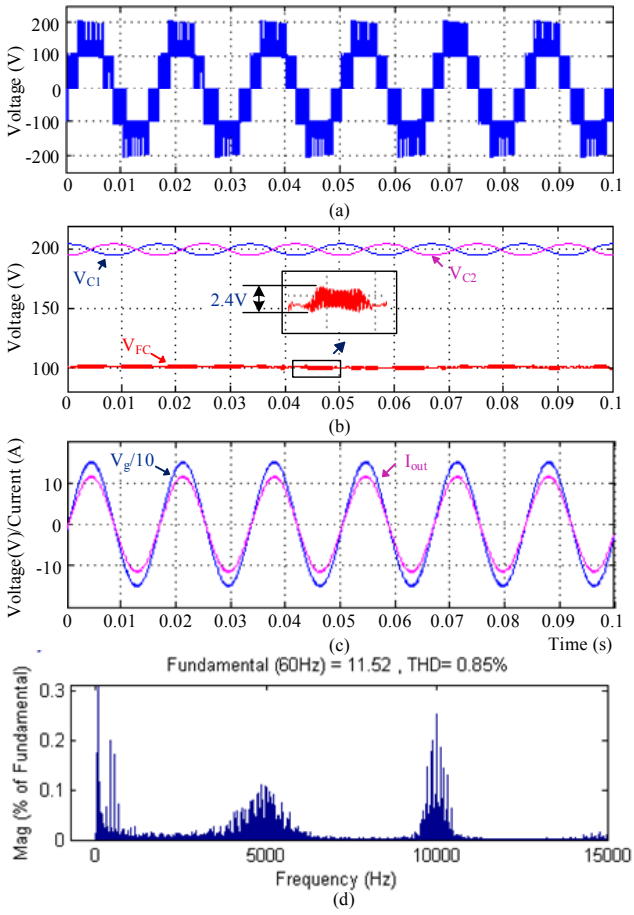

Fig. 8. Simulation results using PS-PWM with the proposed DC balancing technique in steady state. (a) Output voltage. (b) Voltages of three capacitors. (c) Gird voltage and output current. (d) THD of output current.

V. EXPERIMENT VERIFICATOIN

A 1 kW single-phase 7S-5L-ANPC inverter grid-connected laboratory prototype is built to verify the effectiveness of two DC balancing techniques. The experimental setup is shown in Fig. 9. The experimental parameters are identical to the ones used in simulation section, which are shown in Table III.

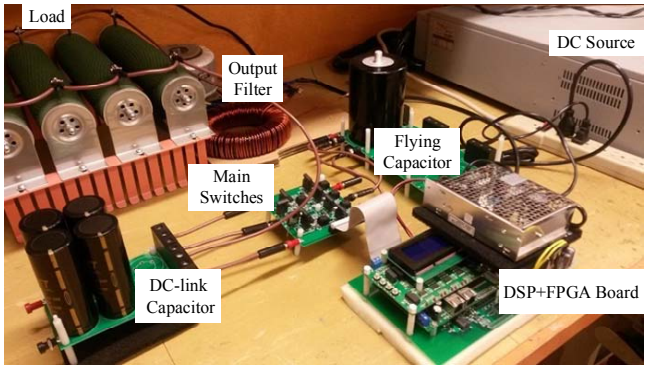

Fig. 9. Experimental prototype.

Fig. 10 shows the inverter output voltage, DC-link capacitor voltages and FC voltage using PS-PWM with the proposed DC balancing technique in unbalanced DC-link capacitor voltages condition. It is observed that, after the dynamic transition, two DC-link capacitor voltages are balanced in 200 V, and the FC voltage is also balanced in 100 V.

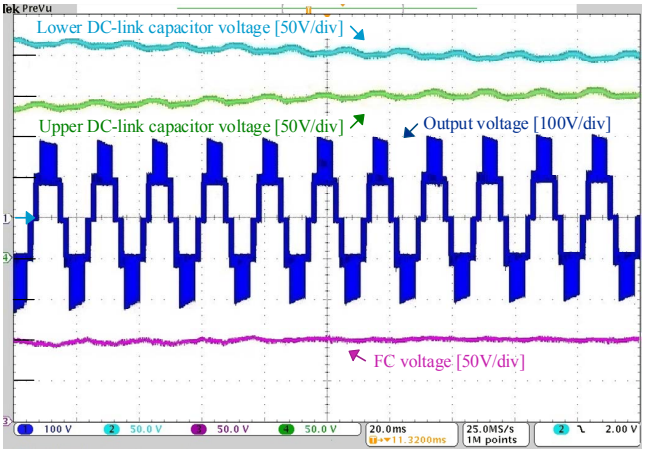

Fig. 10. Experimental results with the proposed DC balancing technique in unbalanced DC voltage condition: waveforms of lower DC-link capacitor voltage, upper DC-link capacitor voltage, bridge voltage and FC voltage.

Fig. 11 and Fig. 12 show the experimental waveforms in steady state using PS-PWM with the proposed DC balancing technique. In Fig. 11, it is observed that FC voltage is balanced in a quarter of the input voltage which is 100 V. The measured FC voltage ripple is 2.9 V (= 2.9 V/100 V = 2.9 %). The output current is sinusoidal without distortion and in phase with grid voltage. The measured output current THD is 1.01 %. In Fig. 12, it is observed that two DC-link capacitor voltages are balanced in 200 V. The measured DC-link capacitor voltage ripple is 15 V (= 15 V/200 V = 7.5 %).

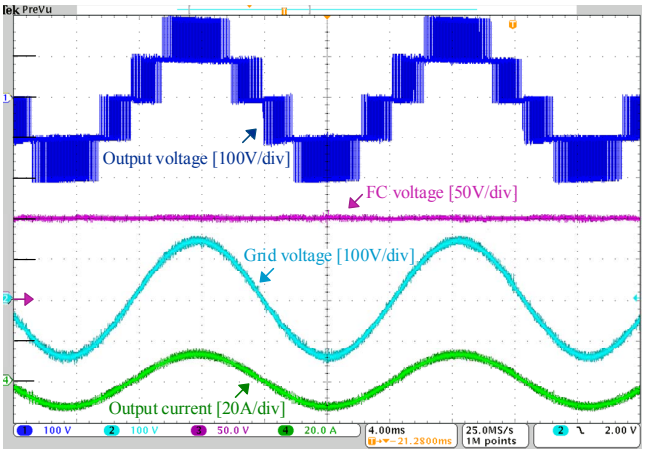

Fig. 11. Experimental results with the proposed DC balancing technique in steady state: waveforms of bridge voltage, FC voltage, grid voltage and output current.

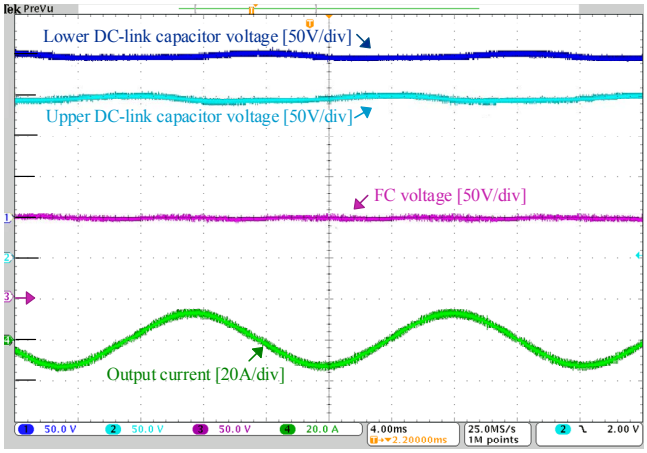

Fig. 12. Experimental results the proposed DC balancing technique in steady state: waveforms of lower DC-link capacitor voltage, upper DC-link capacitor voltage, FC voltage and output current.

VI. Conclusion

In this paper, a new DC-link capacitor voltage balancing techniques for 7S-5L-ANPC inverter using PS-PWM modulation is proposed. The modulation diagram of PS-PWM for 7S-5L-ANPC inverter is given. The power transmission relationship between FC and DC-link capacitors is investigated. With the relationship, the duty cycles of 1 level switching states can be adjusted to balance the DC-link capacitor voltages under PS-PWM. The proposed DC balancing technique can be applied to any 5L-ANPC topologies. The advantages and effectiveness of both techniques are verified by simulation and experimental results.

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