

A High-Efficiency High-Power-Density On-Board Low-Voltage DC–DC Converter for Electric Vehicles Application

Xiang Zhou ¹, Member, IEEE, Bo Sheng, Student Member, IEEE, Wenbo Liu ², Student Member, IEEE, Yang Chen ³, Member, IEEE, Laili Wang ⁴, Senior Member, IEEE, Yan-Fei Liu ⁵, Fellow, IEEE, and Paresh C. Sen, Life Fellow, IEEE

Abstract—The on-board low-voltage dc–dc converter (LDC) in electric vehicles (EVs) is used to connect the high-voltage battery with the low-voltage auxiliary system. With the advancement of auxiliary equipment in EVs, the output current of the LDC can be hundreds of amperes, which will cause high-conduction loss and severe thermal concern. In this article, a high-efficiency high-power-density on-board LDC is presented. To reduce current stress and improve efficiency, three-phase interleaved *LLC* dc–dc converters are paralleled to provide 270 A load current. Synchronous rectifier is used to reduce secondary conduction loss. zero-voltage-switching (ZVS) turn-ON of primary switches and ZCS turn-OFF of secondary switches are achieved, thus switching loss can be reduced significantly. Moreover, phase-shedding technology is used to improve light load efficiency. Switch-controlled capacitor (SCC) technology is used to achieve accurate load current sharing among the three phases, which protects the devices against high-current stress, reduces the conduction loss, and improves the reliability of the system. As SCC switches achieve ZVS turn-ON and turn-OFF by its nature, the loss of the SCC circuit is of less concern with regard to the rated output power. In addition, GaN HEMTs are used in the primary side to improve the power density and eventually help achieving light weight. A 3.8-kW (14 V/270 A) LDC prototype is developed and tested. Experimental results show good current balancing among the three phases. A peak efficiency of 96.7% at 140 A load and a full load efficiency of 95.8% are achieved with 3 kW/L power density and 1.5 kg weight.

Index Terms—Electric vehicles (EVs), *LLC* dc–dc converter, switch-controlled capacitor (SCC), synchronous rectifier (SR).

I. INTRODUCTION

WITH increasing environmental pollution caused by green-house gas emissions from conventional fossil

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Xiang Zhou and Laili Wang are with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: pecel_zhouxiang@163.com; llwang@mail.xjtu.edu.cn).

Bo Sheng, Wenbo Liu, Yang Chen, Yan-Fei Liu, and Paresh C. Sen are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: bo.sheng@queensu.ca; liu.wenbo@queensu.ca; yang.chen@queensu.ca; yanfei.liu@queensu.ca; senp@queensu.ca).

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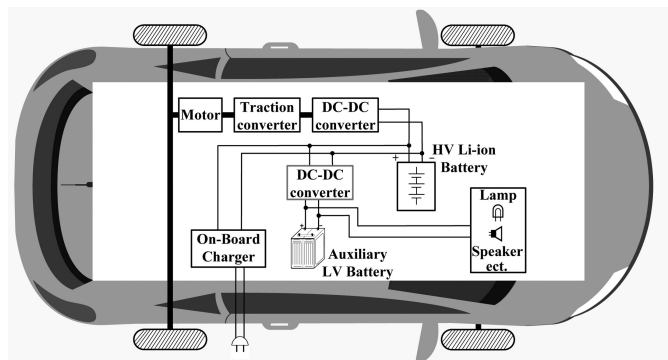


Fig. 1. Diagram of EV power train.

fuel-driven vehicles, electric vehicles (EVs) are attracting increased attention as they are not only more environmentally friendly, but cheaper than fossil fuels vehicles [1]. Along with the development of EVs, more and more auxiliary equipment, e.g., air conditioning, is required to satisfy consumer requirements. The high-power on-board low-voltage dc–dc converter (LDC) is essential in EVs, which takes responsibility to transfer power from high-voltage battery to auxiliary equipment and low-voltage battery. As shown in Fig. 1, the battery system of EVs consists of high voltage (HV) Li-ion batteries (250–430 V) and low voltage (LV) Lead-acid batteries (9–16 V). In general, HV batteries are used for traction of motor drives. LV batteries provide power for auxiliary equipment. As more and more auxiliary equipment is implemented in EVs to provide various additional features nowadays, such as lighting, audio/video systems, air conditioners, automatic seats, sunroofs, and heated seats, high load current level of LDC is the trend. From [1] and [2], at least 2.4 kW power rating is required to supply auxiliary equipment. Therefore, the LDC should output more than 200 A load at 12 V.

Typically, the EVs charger system operates at two modes. First, the HV battery is charged from the grid by the off-board charger or the on-board charger when the vehicle is connected to the grid. Second, the HV battery provides power to auxiliary electronic devices or charges the LV battery through LDC when the vehicle is running [1]. In general, the voltage range of HV battery and the LV battery system is wide. Galvanically isolated

dc–dc converters are required in LDC to ensure safety and obtain high step-down voltage ratio (430–9 V). Moreover, high power-density and light weight are desirable for LDC due to the limitation on space and weight for EVs. Last but not least, high efficiency is required to extend the mileage per charge and to reduce the heatsink size.

In [1], the phase-shift full-bridge converter is adopted in LDC. However, it is difficult to achieve ZVS for the lagging arm under light load. To guarantee ZVS of primary switches in LDC based on the phase-shift full-bridge converter, auxiliary inductors are used in [2]–[4]. In [5], a built-in buck circuit is used in transformer secondary of LDC to solve the induced voltage caused by the multiwinding high-frequency transformer.

In [1]–[7], the phase-shift full-bridge converter is adopted for LDC, and current-doubler circuit is utilized in the transformer secondary to provide high load current [1]–[3], [6]. However, compared to a phase-shift full-bridge dc–dc converter, the resonant converter such as *LLC* dc–dc converter benefits from that ZVS of primary switches and ZCS of secondary switches can be achieved, which is used widely in various application to achieve high-efficiency and high power-density [8]–[13].

In [14]–[17], the *LLC* dc–dc converter is adopted in LDC of EVs. As output current is high in LDC, transformer secondary conduction loss is predominant. Thus, the efficiency could be improved significantly by using the synchronous rectifier (SR) *LLC* dc–dc converter in [14]–[15]. To reduce transformer secondary current stress, the two-phase interleaved *LLC* dc–dc converter is used, and phase-shedding technology is adopted to improve light load efficiency in [16]. Knabben *et al.* [17] utilize both *LLC* and boundary/discontinuous conduction mode (B/DCM) control schemes to improve efficiency and power density.

Multiphase dc–dc converters connected in parallel can help reduce the current stress, which makes an effective way to improve the efficiency. However, for the LDC based on the *LLC* resonant converter, when switching frequency is close to series resonant frequency, the impedance of L_r and C_r in series is close to zero. Small tolerance on L_r or C_r will cause large impedance difference among different phases; thus, the load current would be unbalanced severely and induce uneven heating of the circuit components. If current sharing cannot be achieved in multiphase resonant dc–dc converters connected in parallel, one of the phases may carry all the output current and the other phases may carry no output current. This will degrade the efficiency, increase the current stress and even damage the board. Therefore, current sharing problem needs to be solved to improve the efficiency and reliability.

In [16], two separate voltage loop controllers are utilized in two-phase *LLC* dc–dc converters connected in parallel, which makes two-phase current sharing by operating two phases at the different switching frequency. However, the different switching frequencies will cause beat frequency, which deteriorates the performance of the converter. In [18], two extra auxiliary pulsewidth modulation (PWM) dc–dc converters are used to make two-phase *LLC*-DC-Transformer (DCX) input current sharing. By transforming the current sharing of the resonant converter into PWM control of a dc–dc converter, this method is simple to implement. However, to make sure that the PWM

converter only processes small partial power, the components tolerance of two DCX should be very small.

Current sharing can also be achieved by using series connection in the multiphase *LLC* converter with small resonant components tolerance [19]–[23]. Moreover, the three-phase *LLC* dc–dc converter with Y connection or Δ connection is also confirmed to achieve current sharing by series connection [21]–[23]. However, a serious current imbalance still occurs if large resonant component tolerance presents in the three-phase *LLC* dc–dc converter. In addition, all three phases need to operate at the same time even with light load, thus, the light load efficiency will be degraded.

Compared to multiphase *LLC* dc–dc converters connected in parallel directly, rms input voltage of the resonant tank is lower in the three-phase *LLC* dc–dc converter with Y connection or Δ connection. The current stress of primary components in the three-phase *LLC* dc–dc converter with Y connection or Δ connection is higher under the same specification and the number of switches, which increases conduction loss. Therefore, multiphase *LLC* dc–dc converters connected in parallel have the following advantages: 1) low current stress can reduce the conduction loss; 2) unneeded phases can be shut down to improve the efficiency in light load condition.

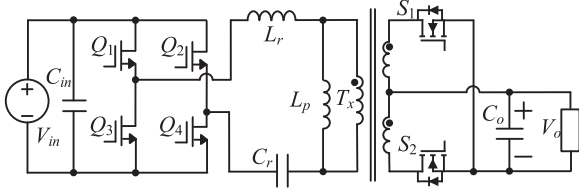
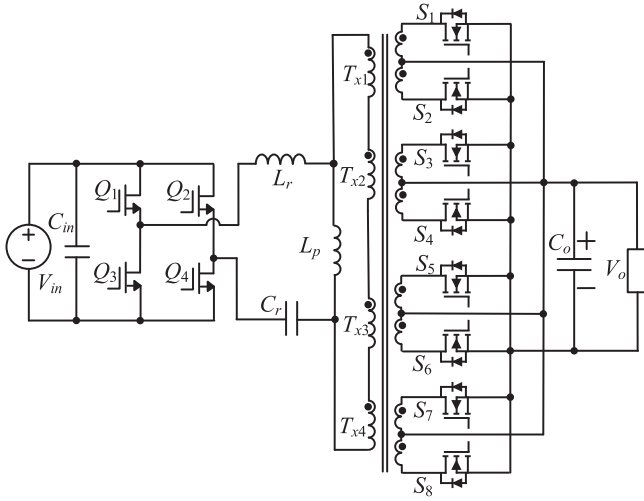
To implement current sharing in multiphase *LLC* dc–dc converters connected in parallel with the same switching frequency, several methods have been proposed in [24]–[30]. By adding capacitor, inductor, etc., passive impedance network so that the impedance of the resonant tanks is matched, a good performance of current sharing is achieved in [24]–[27]. In [28]–[30], magnetic-coupling is adopted to achieve three-phases current sharing. However, to achieve a good current sharing performance, all these methods [21]–[30] required small resonant components tolerance. Otherwise, these methods will become ineffective.

The switch-controlled-capacitor (SCC) method is proposed in [31] to modify the resonant capacitor value so that resonant components tolerance can be compensated and current sharing among phases can be obtained. In [32]–[35], SCC technology has been verified in the resonant dc–dc converter to achieve current sharing. Compared with conventional current sharing approaches, SCC technology can achieve current sharing accurately even under large tolerance among phases.

This article proposes a high-efficiency and high-power-density LDC in EVs application by using a three-phase interleaved *LLC* dc–dc converter. The novelty of the proposed LDC lies in the following:

- 1) reducing the current stress and conduction loss by the proper LDC circuit configuration design;
- 2) SCC circuit is used and current sharing accurately is achieved in three-phase *LLC* dc–dc converters at the same switching frequency even when the three-phase converters have large resonant components tolerance;
- 3) the phase-shedding capability is realized to improve light load efficiency.

Therefore, high efficiency of wide operating range and high power-density is very promising in the proposed LDC, which benefits from balanced and low current stress, phase-shedding


 Fig. 2. Single-phase *LLC* converter.

 Fig. 3. Single-phase *LLC* converter with four transformers series-input parallel-output in [17] and [36].

capability, soft switching of switches in the *LLC* converter and SCC circuit, low-conduction loss of the SCC circuit switches by using the novel modulation strategy, and GaN HEMTs are used as primary side switches.

In this article, Section II illustrates the circuit configuration and conduction loss analysis. Current sharing technology is given in Section III. Section IV presents the parameters selection of the resonant components, and Section V gives the optimal design of the LDC. Experimental results and conclusion are given in Sections VI and VII.

II. ANALYSIS OF THE LDC CONFIGURATION

According to the specification of the proposed LDC, the full-load current is 270 A at 14 V output. If the single-phase *LLC* converter is used as shown in Fig. 2, 270 A load current would flow through SR switches S_1 and S_2 . The conduction loss on the secondary side would be prohibitively high.

To reduce the transformer secondary conduction loss, the authors in [17] and [36] propose the circuit configuration that using four transformers with series-input parallel-output to reduce the current stress of transformer secondary, as shown in Fig. 3. However, only one-phase full-bridge inverter and resonant components are used in transformer primary, conduction loss would also be large at heavy load.

Instead of using one phase on the transformer primary side, several phases parallel connection topology can be used to provide high load current. Taking three-phase parallel connection

TABLE I
COMPARISON OF LOSS IN DIFFERENT FULL-BRIDGE *LLC* DC-DC CONVERTER STRUCTURE

Structure	1 modular in Fig. 2	1 modular in Fig. 3	3 modular in parallel in Fig. 4
Transformer	1 transformer	4 transformers series-input parallel-output	2 transformers series-input parallel-output in each modular
RMS current of primary switches	$\frac{\pi V_o}{4V_{in}} \times I_o$ = 7.8A	$\frac{\pi V_o}{4V_{in}} \times I_o$ = 7.8A	$\frac{\pi V_o}{12V_{in}} \times I_o$ = 2.6A
RMS current of L_r	$\frac{\pi V_o}{2\sqrt{2}V_{in}} \times I_o$ = 11.0A	$\frac{\pi V_o}{2\sqrt{2}V_{in}} \times I_o$ = 11.0A	$\frac{\pi V_o}{6\sqrt{2}V_{in}} \times I_o$ = 3.7A
RMS current of SR switches	$\frac{\pi}{4} I_o = 212.1A$	$\frac{\pi}{16} I_o = 53.0A$	$\frac{\pi}{24} I_o = 35.3A$
Total conduction loss of primary switches	$\frac{\pi^2 R_{ds,QP} V_o^2}{4V_{in}^2} \times I_o^2$ = 24.3W	$\frac{\pi^2 R_{ds,QP} V_o^2}{4V_{in}^2} \times I_o^2$ = 24.3W	$\frac{\pi^2 R_{ds,QP} V_o^2}{12V_{in}^2} \times I_o^2$ = 8.1W
Total copper loss of L_r and transformer primary	$\frac{\pi^2 V_o^2 (R_{Lr} + R_{Tx-p})}{8V_{in}^2}$ $\times I_o^2 = 16.9W$	$\frac{\pi^2 V_o^2 (R_{Lr} + 4R_{Tx-p})}{8V_{in}^2}$ $\times I_o^2 = 40.5W$	$\frac{\pi^2 V_o^2 (R_{Lr} + 2R_{Tx-p})}{72V_{in}^2}$ $\times I_o^2 = 2.8W$
Total copper loss of transformer secondary and conduction loss of SR switches	$\frac{\pi^2 (R_{ds,SR} + \frac{R_{Tx-s}}{2})}{8}$ $\times I_o^2 = 112.5W$	$\frac{\pi^2 (R_{ds,SR} + \frac{R_{Tx-s}}{2})}{32}$ $\times I_o^2 = 28.1W$	$\frac{\pi^2 (R_{ds,SR} + \frac{R_{Tx-s}}{2})}{48}$ $\times I_o^2 = 18.7W$
Total conduction loss and the percentage of output power	153.7W (4.1%)	92.9W (2.5%)	29.6W (0.78%)

as an example, each *LLC* converter needs to provide 90 A out of 270 A load current, as shown in Fig. 4. Thus, each phase can be designed based on 1/3 load conditions, which will help improve the efficiency. Moreover, phase-shedding technology can be applied to further improve the light load efficiency. When two transformers are adopted in each phase with input-series output-parallel, each transformer needs to process only 45 A load current.

Based on the abovementioned assumption, the comparison of the rms current and copper loss is given in Table I at $V_{in} = 380$ V, $V_o = 14$ V, and $I_o = 270$ A. For the convenience of the comparison, several assumptions are made in Table I, i.e., the on-state resistance of SRs is $R_{ds,SR} = 0.5$ m Ω , the on-state resistance of primary switches is $R_{ds,QP} = 100$ m Ω , the resistance of transformer primary is $R_{Tx-p} = 65$ m Ω , the resistance of transformer secondary is $R_{Tx-s} = 1.5$ m Ω and the equivalent series resistance of inductor L_r is $R_{Lr} = 75$ m Ω . Core loss and switching loss are not considered as they do not change too much with the current.

According to Table I, the transformer primary currents stress of the circuits in Figs. 2 and 3 both are three times of that in Fig. 4; and the transformer secondary current stress of the circuit in Fig. 2 is six times that in Fig. 4. As the conduction loss is related to the square of rms current, the copper loss and conduction loss of the circuit in Fig. 4 are reduced significantly.

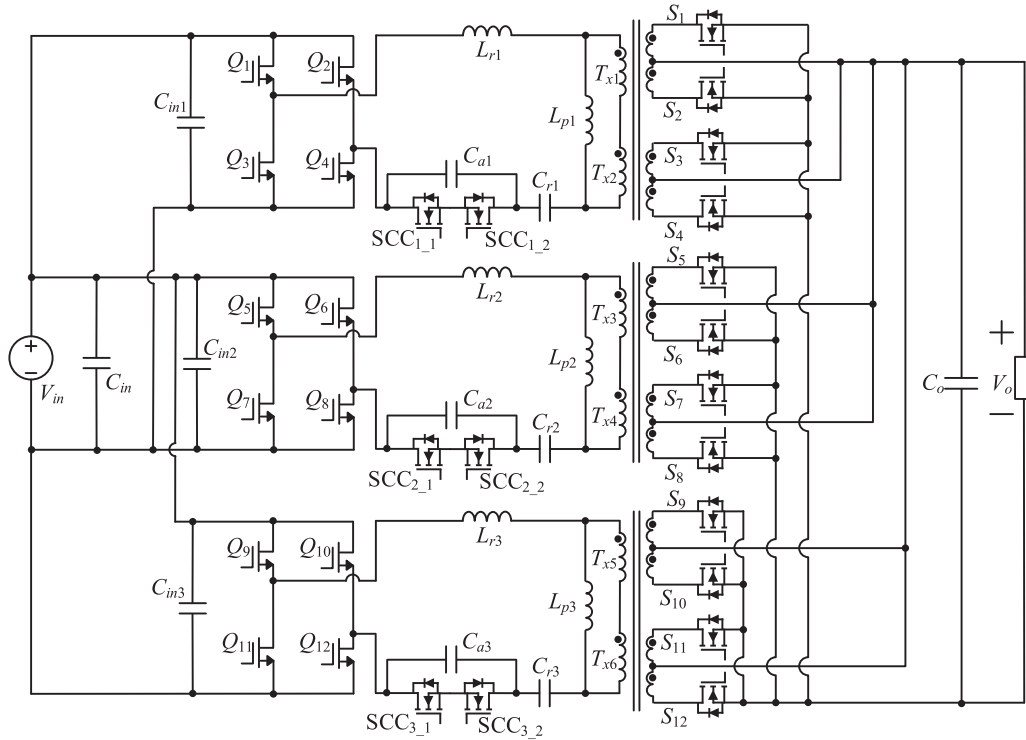


Fig. 4. Circuit configuration of the proposed three-phase *LLC* converter with SCC circuit for LDC.

TABLE II
COMPARISON OF DIFFERENT 650 V SWITCHES

GSS66508		IPL65R099C7		IPL65R070C7	
Q_g	5.8nC	Q_g	45nC	Q_g	64nC
$R_{ds(on)}$ @ $T_j=100^\circ\text{C}$	102m Ω	$R_{ds(on)}$ @ $T_j=100^\circ\text{C}$	165m Ω	$R_{ds(on)}$ @ $T_j=100^\circ\text{C}$	118m Ω
Package	GaN _{PX}	Package	PG-VSON-4	Package	PG-VSON-4
Driver loss @6V 500kHz	17.4mW	Driver loss @10V 500kHz	225mW	Driver loss @10V 500kHz	320mW
Conduction loss@ $I_{ds,RMS}=3\text{A}$	918mW	Conduction loss@ $I_{ds,RMS}=3\text{A}$	1485mW	Conduction loss@ $I_{ds,RMS}=3\text{A}$	1062mW
Total (12 switches)	11.22W	Total (12 switches)	20.52W	Total (12 switches)	16.58W

Compared to the three-phase converters shown in Fig. 4, the single-phase topology in Fig. 2 produces 124.1 W extra loss, which will cause 3.3% efficiency degrading at 14 V and 270 A output and bring difficulty to the cooling system.

To reduce conduction loss and improve efficiency, the proposed LDC for EVs adopts three-phase interleaved *LLC* dc–dc structure. Moreover, two transformers with input-series output-parallel are used in each phase *LLC* dc–dc converter to further reduce the secondary side SR conduction loss.

Since the switching frequency is high to improve the power density for the proposed LDC, GaN HEMTs are used as the primary side switches to reduce the primary switches loss. The comparison of different 650 V switches is shown in Table II. The power loss of GaN HEMT: GSS66508, Silicon MOSFETS:

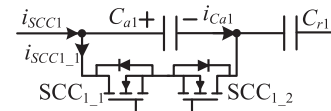


Fig. 5. SCC circuit in the first phase of the proposed LDC.

IPL65R099C7 and IPL65R070C7 as primary side switches are compared. Thanks to the low Q_g and $R_{ds(on)}$, GaN HEMT could help reduce the power loss by 5–9 W.

III. ANALYSIS OF THE SCC CIRCUIT

A. Proposed LDC With SCC Technology

As aforementioned analysis, three *LLC* converters connected in parallel can reduce the power loss. However, impedance mismatch caused by the tolerance of the resonant components in different phases will lead to current sharing problem in multiphase converters, which degrades the benefits achieved by the parallel techniques. This article uses an SCC circuit to achieve current sharing among three-phases accurately, and the proposed LDC with SCC circuit is shown in Fig. 4. Three SCC circuits are added into each phase to achieve current sharing.

The equivalent resonant capacitor value can be adjusted to achieve current sharing among three *LLC* dc–dc converters even under large resonant components tolerance.

Fig. 5 shows the SCC circuit in the first phase of the proposed LDC. The capacitor C_{a1} is connected in parallel with the switches S_1 and S_2 . If switches S_1 and S_2 are turned ON, capacitor C_{a1} is shorted. If switches S_1 and S_2 are turned OFF, capacitor

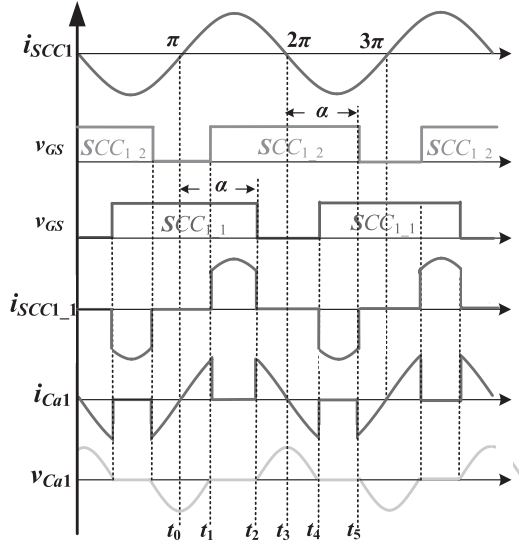


Fig. 6. Control strategy of SCC circuit in this article.

C_{a1} is in series with capacitor C_{r1} , and the equivalent resonant capacitor $C_{r,eq}$ is smaller than C_{r1} .

To reduce the loss of SCC circuit in [32]–[35], the control strategy of SCC circuit shown in Fig. 6 is adopted in this article. Defining that α represents delay phase angle of SCC switches with regard to the current crossover point, as shown in Fig. 6. Assuming that a sinusoidal current i_{SCC1} flows through the SCC circuit, the zero-crossing points of current i_{SCC1} are at angle 0, π , 2π ..., etc. For a positive half cycle, the switch SCC_{1-2} is turned ON at angle $2n\pi - \alpha$ and turned OFF at angle $2n\pi + \alpha$, switch SCC_{1-1} is turned ON at angle $(2n+1)\pi - \alpha$ turned OFF at angle $(2n+1)\pi + \alpha$. In the actual implementation, the SCC MOSFET is turned OFF α degree after zero-crossing point of the resonant current. The SCC MOSFET is turned ON when the voltage across C_a reduced to zero. Since the capacitance of C_a is large in the real application, such as 10 nF, the voltage V_{Ca} increases slowly, leading to ZVS turn-OFF for SCC_{1-1} . After C_a is fully discharged at t_4 , SCC_{1-1} is turned ON and achieved ZVS turn-ON when the capacitor voltage drops to zero. Similarly, switch SCC_{1-2} can also achieve ZVS turn-ON and turn-OFF.

Taking the first-phase circuit as an example, from [31], the equivalent capacitance of SCC circuit can be calculated as

$$C_{SCC,phase\ 1} = \frac{C_{a1}}{2 - (2\alpha - \sin 2\alpha)/\pi}. \quad (1)$$

From Fig. 5 and (1), the equivalent resonant capacitor $C_{r,eq}$ is

$$C_{r,eq} = \frac{C_{SCC,phase\ 1} C_{r1}}{C_{SCC,phase\ 1} + C_{r1}}. \quad (2)$$

Taking SCC circuit into consideration, the voltage gain of the first-phase circuit in the proposed LDC becomes

$$M = \frac{2nV_o}{V_{in}} = \frac{K}{\sqrt{[(\frac{\omega_r}{\omega_s})^2 - K - 1]^2 + \frac{(\pi^2 \omega_s L_{p1})^2}{64n^4 R_L^2} [(\frac{\omega_r}{\omega_s})^2 - 1]^2}} \quad (3)$$

where R_L is load resistance of the first phase, $K = L_{p1}/L_{r1}$, $\omega_s = 2\pi f_s$, and $\omega_r = 1/\sqrt{L_{r1}C_{r,eq}}$. Similarly, the second and third phase have the same voltage gain shown in (3) when the same resonant parameters are selected.

In the LLC dc-dc converter, the resonant components parameters are always designed with the assumption that there is no tolerance among multiphases circuits. According to (1) and (2), a large α has small effect on the resonant parameters of the LLC converter. Therefore, in the proposed LDC, delay angles of all three phases SCC switches α are set to the maximum value α_{max} at the beginning. If there is tolerance among three phases, SCC circuit will compensate the resonant parameters and make three-phase current sharing by adjusting α .

From (3), the load currents of three phases can be shared by adjusting the delay angle α of switches SCC_{1-1} – SCC_{3-2} so that three-phase circuits have the same voltage gains at the same switching frequency. Therefore, the total input current and load current will be distributed into three phases equally even if the three-phase converters have large resonant components tolerance.

B. Loss Analysis of SCC Circuit

In the SCC circuit, from Fig. 6, the rms current flowing through SCC switches $I_{SCC1-1,RMS}$ is

$$I_{SCC1-1,RMS} = \sqrt{\frac{\int_{\pi-\alpha}^{\alpha} [\sqrt{2}I_{Lr1,RMS} \sin(t)]^2 dt}{\pi}} = I_{Lr1,RMS} \sqrt{\frac{2\alpha}{\pi} - \frac{\sin 2\alpha}{\pi} - 1}. \quad (4)$$

The average absolute value of the current flowing through SCC switches I_{SCC1-1,AVE_ABS} is

$$I_{SCC1-1,AVE_ABS} = \frac{\int_{\pi-\alpha}^{\alpha} \sqrt{2}I_{Lr1,RMS} \sin(t) dt}{\pi} = \frac{-2\sqrt{2}I_{Lr1,RMS}}{\pi} \cos \alpha. \quad (5)$$

As ZVS turn-ON and turn-OFF are achieved, there is only conduction loss of two SCC switches. The current i_{SCC1-1} flows through one MOSFET and one body diode of MOSFET in the control strategy of [32]–[35], thus, the loss of one SCC circuit in [32]–[35] is

From Figs. 5 and 6, current i_{SCC1-1} flows through two MOSFETs in this work, thus, the loss of one SCC circuit in the proposed LDC is

$$P_{loss,SCC\ in\ this\ work} = 2R_{ds(on)}I_{SCC1-1,RMS}^2 = 2I_{Lr1,RMS}^2 \left(\frac{2\alpha}{\pi} - \frac{\sin 2\alpha}{\pi} - 1 \right)^2 R_{ds(on)}. \quad (7)$$

According to (6) shown at the bottom of this page and (7), the loss of one SCC circuit against delay angle α with different resonant current $I_{Lr1,RMS}$ in [32]–[35] and in this work is shown in Fig. 7. As three SCC circuits are used in the proposed LDC, if $I_{Lr1,RMS} = 4$ A and $\alpha = 160^\circ$, the total loss of three SCC

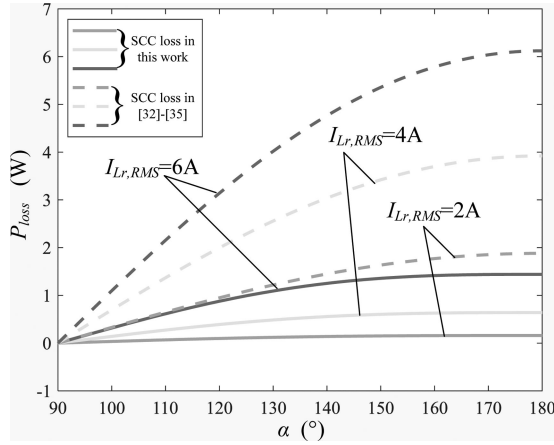


Fig. 7. Loss comparison of the SCC circuit.

switches is 11.1 W in [32]–[35], while the total loss of three SCC switches is only 1.9 W in this work, which can help reduce the power loss by 9.2 W.

IV. PARAMETERS DESIGN OF THE LDC

Since the three-phase *LLC* dc–dc converters have the same parameters design in the proposed LDC, only taking the first phase-circuit analysis as an example. To ensure the converter operates in the ZVS region of primary switches and ZCS region of the SR, the resonant point (unity voltage gain) is selected based on the maximum input voltage and the minimum output voltage. The transformer turns ratio is determined by

$$n = N_p : N_s = V_{in_max} : V_{o_min} \quad (8)$$

where N_p is the primary turns number and N_s is the secondary turns number.

With 430 V maximum input and 9 V minimum output voltage, each transformer turns ratio should be $430 \text{ V} / 9 \text{ V} / 2 = 23.8$. However, as 9 V is an odd point with less current requirement, the turns ratio is selected as 22:1:1 for each transformer.

For EVs, the maximum output power of the LDC is limited by the voltages across HV battery. In this case, load capacity is different at different input and output conditions. Each phase of the *LLC* dc–dc converter considers maximum $90 \text{ A} \times 14 \text{ V} = 1260 \text{ W}$ load for resonant parameter design. For 330–430 V input voltage, the converter is rated for full power; while for 250–330 V input voltage, only 60% load is needed. In the proposed LDC, wide input voltage (250–430 V) and output voltage (9–16 V) range are required. Because 250 V input and 16 V output is maximum step-up voltage gain point, the design of the resonant parameters should satisfy this condition. As only 60% load is needed at 250 V input voltage, voltage gain should satisfy

Case 1:

$$M = \frac{nV_o}{V_{in}} = \frac{16 \times 44}{250} = 2.82 \quad (9)$$

in this case, for each phase, quality factor Q satisfies

$$\begin{aligned} Q &= \frac{\pi^2 I_o / 3}{8n^2 V_o} \sqrt{\frac{L_{r1}}{C_{r1}}} = \frac{\pi^2 \times (90 \times 0.6 \times 14 \div 16)}{8 \times 44^2 \times 16} \sqrt{\frac{L_{r1}}{C_{r1}}} \\ &= 1.882 \times 10^{-3} \sqrt{\frac{L_{r1}}{C_{r1}}}. \end{aligned} \quad (10)$$

When the input voltage is 330 V, full load needs to be carried, and the resonant parameters should be designed for this condition. When the output voltage is 16 V, the maximum step-up voltage gain is

Case 2:

$$M = \frac{nV_o}{V_{in}} = \frac{16 \times 44}{330} = 2.13 \quad (11)$$

and quality factor Q satisfies

$$\begin{aligned} Q &= \frac{\pi^2 I_o / 3}{8n^2 V_o} \sqrt{\frac{L_{r1}}{C_{r1}}} = \frac{\pi^2 \times (90 \times 14 \div 16)}{8 \times 44^2 \times 16} \sqrt{\frac{L_{r1}}{C_{r1}}} \\ &= 3.136 \times 10^{-3} \sqrt{\frac{L_{r1}}{C_{r1}}}. \end{aligned} \quad (12)$$

As large Q value would decrease voltage gain, 14 V output 90 A load current should also be considered in this design. When the output voltage is 14 V, the maximum step-up voltage gain is

Case 3:

$$M = \frac{nV_o}{V_{in}} = \frac{14 \times 44}{330} = 1.87 \quad (13)$$

and quality factor Q satisfies

$$\begin{aligned} Q &= \frac{\pi^2 I_o / 3}{8n^2 V_o} \sqrt{\frac{L_{r1}}{C_{r1}}} = \frac{\pi^2 \times 90}{8 \times 44^2 \times 14} \sqrt{\frac{L_{r1}}{C_{r1}}} \\ &= 4.097 \times 10^{-3} \sqrt{\frac{L_{r1}}{C_{r1}}}. \end{aligned} \quad (14)$$

Compared with 100–200 kHz resonant frequency in traditional LDC, the resonant frequency between L_{r1} and C_{r1} is selected to be around 500 kHz to reduce the volume of magnetic components and improve the power density in this work. According to [38], three sets of resonant parameters are selected to meet the parameters design for the proposed LDC, and the accurate voltage gain curves are given in Fig. 8 by using the time-domain analysis method.

As shown in Fig. 8(a), when $K = 3$, $f_r = 546 \text{ kHz}$, $Q = 0.45$, that is $L_{r1} = 32 \mu\text{H}$, $L_{p1} = 96 \mu\text{H}$, and $C_{r1} = 2.7 \text{ nF}$, the maximum voltage gains of the three cases are achievable, and the minimum switching frequency is $0.58f_r$. However, the inductance of L_p is too small, which is difficult to optimize the

$$\begin{aligned} P_{\text{loss,SCC in [32]-[35]}} &= I_{\text{SCC1,1,RMS}}^2 R_{\text{ds(on)}} + I_{\text{SCC1,1,AVE_ABS}} V_F \\ &= I_{Lr1,\text{RMS}}^2 \left(\frac{2\alpha}{\pi} - \frac{\sin 2\alpha}{\pi} - 1 \right)^2 R_{\text{ds(on)}} + \frac{-2\sqrt{2} I_{Lr1,\text{RMS}} V_F}{\pi} \cos \alpha \end{aligned} \quad (6)$$

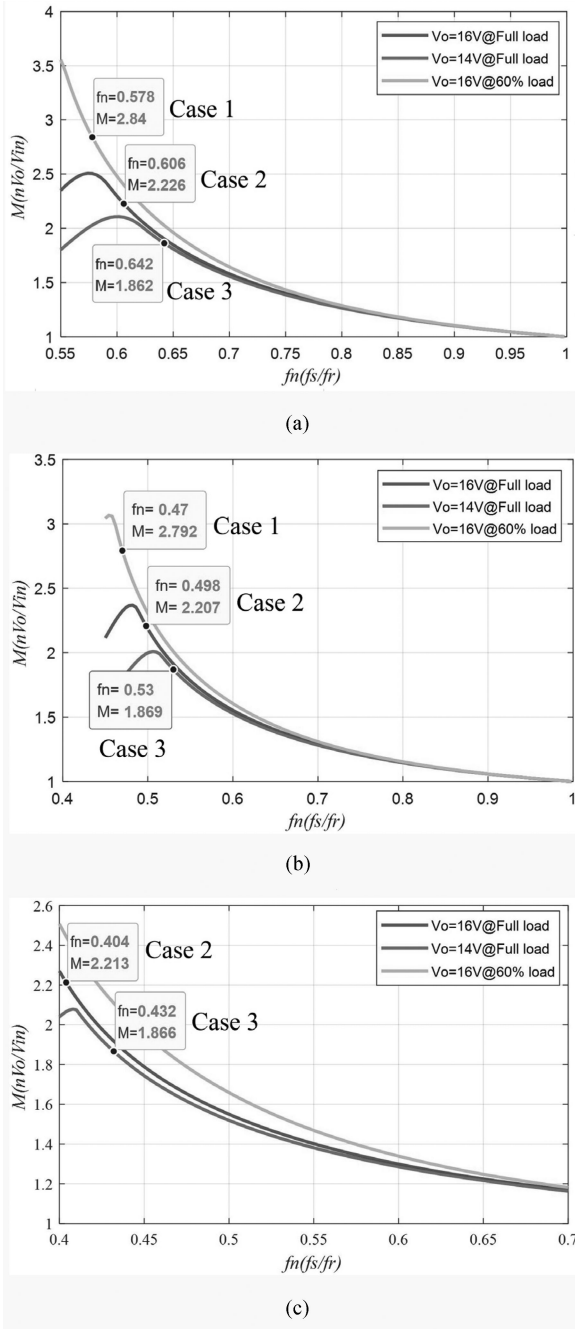


Fig. 8. Voltage gain with different resonant parameters. (a) voltage gain when $K = 3$ and $Q = 0.45$ ($L_{r1} = 32 \mu\text{H}$, $L_{p1} = 96 \mu\text{H}$, $C_{r1} = 2.7 \text{ nF}$). (b) Voltage gain when $K = 5$ and $Q = 0.35$ ($L_{r1} = 25 \mu\text{H}$, $L_{p1} = 125 \mu\text{H}$, $C_{r1} = 3.4 \text{ nF}$). (c) Voltage gain when $K = 8$ and $Q = 0.25$ ($L_{r1} = 18 \mu\text{H}$, $L_{p1} = 142 \mu\text{H}$, $C_{r1} = 4.8 \text{ nF}$).

fringing loss and core loss. As shown in Fig. 8(b), when $K = 5$, $f_r = 546 \text{ kHz}$, $Q = 0.35$, that is $L_{r1} = 25 \mu\text{H}$, $L_{p1} = 125 \mu\text{H}$, and $C_{r1} = 3.4 \text{ nF}$, the maximum voltage gains of the three cases are also achievable, and the minimum switching frequency is $0.47f_r$. As shown in Fig. 8(c), when $K = 8$, $f_r = 546 \text{ kHz}$, $Q = 0.25$, that is $L_{r1} = 18 \mu\text{H}$, $L_{p1} = 142 \mu\text{H}$, and $C_{r1} = 4.8 \text{ nF}$, the maximum voltage gains of the three cases can also be achieved, and the minimum switching frequency is smaller than $0.4f_r$.

If the switching frequency is too far away from the resonant frequency, the efficiency of the converter would not be optimal. As L_{p1} is too small in the first set of resonant parameters and the switching frequency range is too wide in the third set of resonant parameters, the second set of resonant parameters $L_{r1} = 25 \mu\text{H}$, $L_{p1} = 125 \mu\text{H}$, $C_{r1} = 3.4 \text{ nF}$ are selected, and the resonant parameters of the second and third phase are the same as that of the first phase.

V. MAGNETIC COMPONENTS AND PCB DESIGN OF THE PROPOSED LDC

A. Design of Magnetic Components

In this article, the center-tap transformer is used with 22:1:1 turns ratio. As shown in Fig. 4, two transformers primary are in series, if L_{p1} is selected as $125 \mu\text{H}$, $62.5 \mu\text{H}$ magnetizing inductor is needed in each transformer. As at least 22 turns are designed for transformer primary winding, thus, a large air gap is required for the transformers, which means large fringing loss. In the proposed LDC, an external inductor L_{p1} is used so that no air gap is needed for the transformer to improve the efficiency.

If the proposed LDC operates at resonant frequency with 380 V input and 14 V/270 A output, the rms current flowing through one of the transformer secondary side winding is

$$i_{Tx1,s,RMS} = \frac{\pi}{2} \times \frac{I_o/3}{2\sqrt{2}} \times \frac{1}{\sqrt{2}} = 35.3 \text{ A} \quad (15)$$

the rms current of transformer primary winding is

$$i_{Tx1,p,RMS} = \frac{\sqrt{2}i_{Tx1,s,RMS}}{n} = 2.3 \text{ A} \quad (16)$$

the rms current i_{Lp1} is

$$i_{Lp1,RMS} = \frac{2nV_oT}{4L_{p1}} \times \frac{1}{\sqrt{3}} = 1.3 \text{ A} \quad (17)$$

and the rms current i_{Lr1} is

$$i_{Lr1,RMS} = \frac{\pi V_o I_o / 3}{2\sqrt{2}V_{in}} = 3.7 \text{ A}. \quad (18)$$

As the converter operates at a switching frequency higher than 260 kHz, litz wire is used to implement the magnetic components to reduce the ac losses caused by skin effect and proximity effect.

According to the current stress shown in (15)–(18), the different litz wires are selected for the magnetic components. The core size, material, and structure of all the magnetic components are shown in Table III.

Fig. 9 shows the photograph of the primary side and secondary side of the transformer. The primary winding uses 22 turns of two layers of litz wire. On the secondary side, each of the center-tapped windings is created using 1 turn of three paralleled $20 \text{ mm} \times 0.25 \text{ mm}$ copper foils.

B. Design of PCB Board

For the LDC prototype, if only one PCB board is used, magnetic components, controller circuit, and active devices should be placed on the same one board. Thus, the vertical space of the structure is not efficiently used because the height of magnetic

TABLE III
CORE SIZE AND MATERIAL OF MAGNETIC COMPONENTS

Inductor L_{r1}		Inductor L_{p1}		Transformer	
Core Size	PQ32/20	Core Size	PQ35/35	Core Size	PQ35/35
Material	3C97	Material	3C97	Material	3C97
Litz Wire	NELC650/44SN	Litz Wire	NELC1100/48SN	Litz Wire / Copper foil	NELC650/44SN / three-layer laminated 0.25mm copper foil
Turns	15	Turns	44	Turns	22:1:1
Laminated layers	3	Laminated layers	4	Laminated layers	2 (Primary) / 3 (Secondary)
Air gap	1.5mm	Air gap	5mm	Air gap	0mm

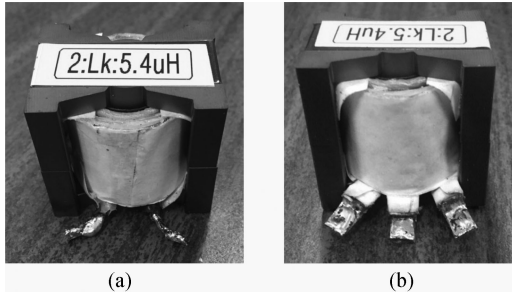


Fig. 9. Photograph of the transformer. (a) Primary side. (b) Secondary side.

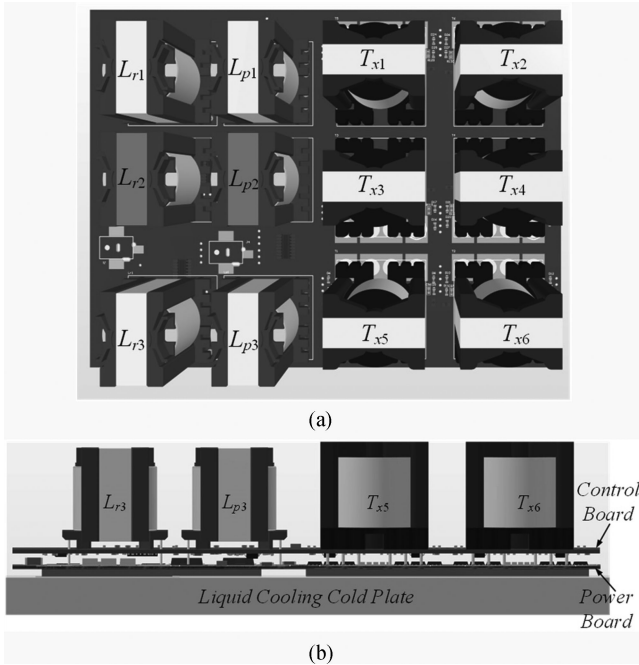


Fig. 10. 3-D Model of the proposed LDC. (a) Top view of the LDC. (b) Front view of the LDC with two PCB liquid cooling assembly.

components is much larger than controller circuit and active devices. The space above the active devices and controller circuit is basically not utilized, which reduces the power density of the converter.

Fig. 10 shows the 3-D model of the proposed LDC. A two-PCB structure is proposed to make full use of the vertical space. The upper PCB is the controller board. MCU, gate driver of switches, etc. are placed on this board. The lower PCB is the

TABLE IV
SPECIFICATIONS AND PARAMETERS OF THE PROPOSED LDC

Input voltage	250V ~ 430V
Output voltage	9V ~ 16V
Maximum output current	270A (90A×3)
Maximum output power	3.8kW
Transformer	$N_p:N_s = 22 : 1$, PQ35/35 core
Parallel inductor	$L_{p1} = 125.3\mu\text{H}$, $L_{p2} = 124.3\mu\text{H}$, $L_{p3} = 124.5\mu\text{H}$, PQ35/35 core
Series inductor	$L_{r1} = 25.6\mu\text{H}$, $L_{r2} = 25.7\mu\text{H}$, $L_{r3} = 25\mu\text{H}$, PQ32/20 core
Series capacitor	C1808C681JGGAC7800 2KV, 680pF × 5 ($\pm 5\%$)
SCC capacitor	C2012NP02W472J125AA, 450V, 4700 pF × 3
Primary switches	GS66508B (650V, 30A)
Secondary switches	TPHR8504PL (40V, 150A)
SCC switches	IPB200N25N3 (250V, 64A)
Input capacitor	C5750X6S2W225K250KA, 450V, $2.2\mu\text{F} \times 18$ + UPZ2W560MHD, 450V, $56\mu\text{F} \times 1$
Output capacitor	C3216JB1E336M160AC, 25V, $33\mu\text{F} \times 10$ + UHE1E331MPD, 25V, $330\mu\text{F} \times 2$
Micro-controller	DSPIC33FJ32GS610

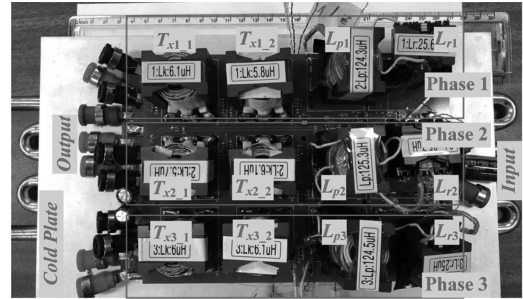


Fig. 11. Prototype of the proposed LDC.

power board. Primary GaN HEMTs, SCC switches and SR switches are placed on this board. Between the two parallel PCBs, a short distance is designed to place the devices. Magnetic components are placed on top of the control board (top board). The pins of the magnetic components are connected to the power board (bottom board) by metal connectors. The liquid cooling cold plate is connected to the bottom side of the power PCB to maximize the cooling performance on active devices to dissipate heat. Thus, high power-density is achieved in this design.

VI. EXPERIMENTAL RESULTS

To verify the analysis, a 3.8-kW LDC prototype is built and tested. The series resonant inductor is $25\mu\text{H}$, the parallel inductor is $125\mu\text{H}$, the resonant capacitor is 3.4 nF , the SCC capacitor is 14 nF , and the transformer turns ratio is $n_p:n_{s1}:n_{s2} = 22:1:1$. The specifications and parameters of the proposed LDC are given in Table IV.

Figs. 11 and 12 show the prototype of the proposed LDC and the test bench. The prototype with 3 kW/L power-density and 1.5 kg weight is achieved. In the proposed LDC, three interleaved *LLC* converters are paralleled for reducing the current stress to improve the efficiency, and the SCC circuit is used to make sure three-phase current sharing. The liquid cooling is used for heat dissipation of the devices on the main board, and the fan cooling

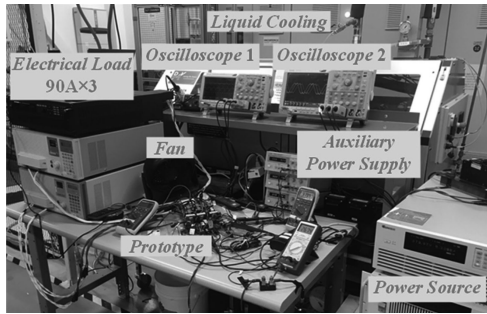


Fig. 12. Test bench.

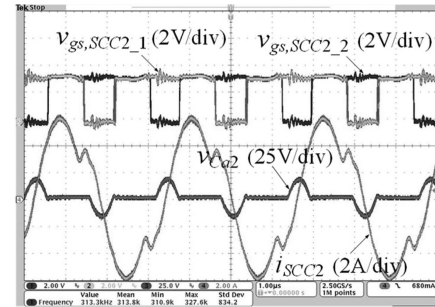
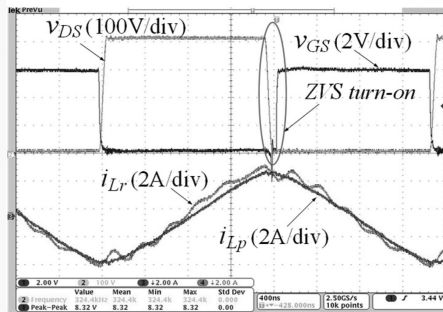
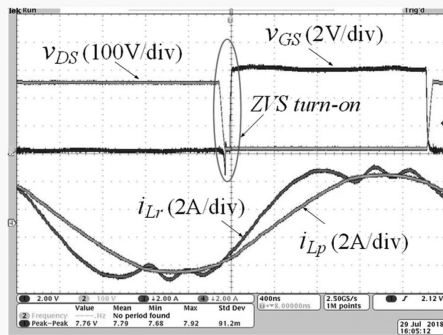


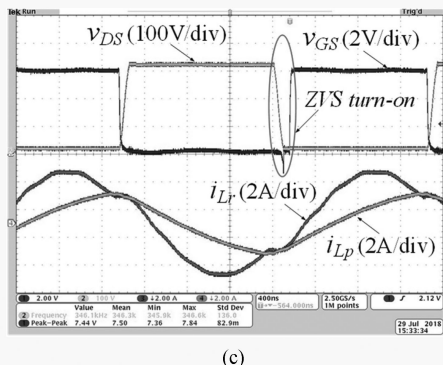
Fig. 14. Waveform of the second-phase SCC circuit at 380 V input and 14 V/90 A output.



(a)



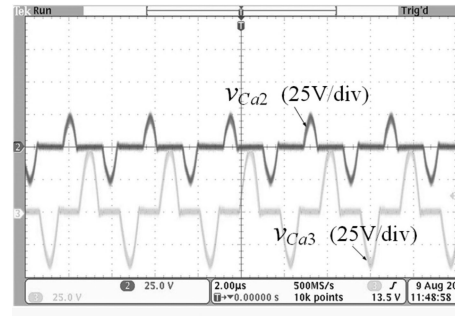
(b)



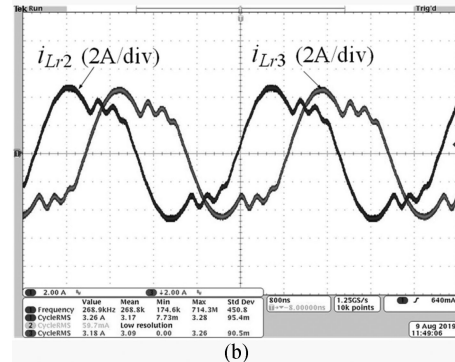
(c)

Fig. 13. Waveforms of v_{gs} , v_{ds} of primary switches and current i_{Lr} , i_{Lp} in single-phase circuit, (a) at 430 V input and 14 V output with 5 A load current, (b) at 250 V input and 16 V output with 40 A load current, (c) at 330 V input and 9 V output with 70 A load current.

is used for heat dissipation of the magnetic components. Three 90 A electronics load is paralleled to provide 270 A load. In practice, the highest current tested is 260 A due to the power limitation of the electronic load.



(a)



(b)

Fig. 15. Waveforms of two-phase circuits operation at 250 V input, 14 V/100 A output. (a) SCC capacitor voltage v_{Ca2} and v_{Ca3} . (b) Resonant current i_{Lr2} and i_{Lr3} .

As shown in Fig. 13, a wide voltage range 250–430 V input and 9–16 V output is achieved. In Fig. 13(a), input and output voltages are 430 and 14 V with 5 A load current, and the switching frequency is 324 kHz. In Fig. 13(b), input and output voltages are 250 and 16 V with 40 A load current, and the switching frequency is 260 kHz. In Fig. 13(c), input and output voltages are 330 and 9 V with 70 A load current, and the switching frequency is 346 kHz. From Fig. 13, ZVS turn-ON can be achieved in light and heavy load at a wide switching frequency range.

As shown in Fig. 14, input and output voltage are 380 V and 14 V when the load of the second-phase circuit is 90 A, delay angle α is 149°. From Fig. 14, ZVS turn-ON and ZVS turn-OFF can be achieved, and the voltage stress of the switches in SCC circuit is low (around 25 V), which verifies the analysis.

Fig. 15 shows the waveforms of the SCC current sharing technology is used in the proposed LDC. When the second and

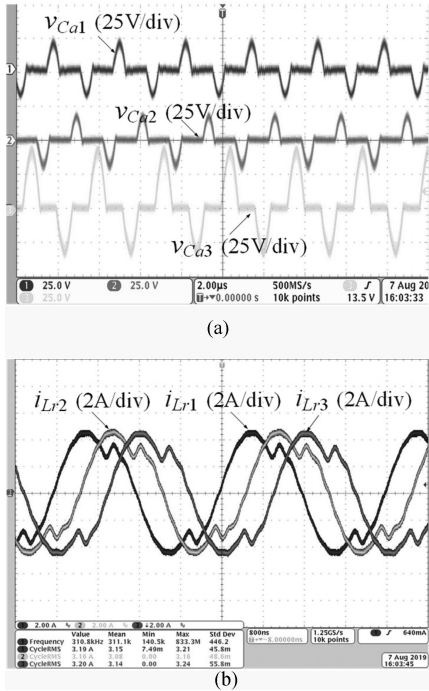


Fig. 16. Waveforms of three-phase circuits operation at 380 V input, 14 V/200 A output. (a) SCC capacitor voltage v_{Ca1} , v_{Ca2} , and v_{Ca3} . (b) Resonant current i_{Lr1} , i_{Lr2} , and i_{Lr3} .

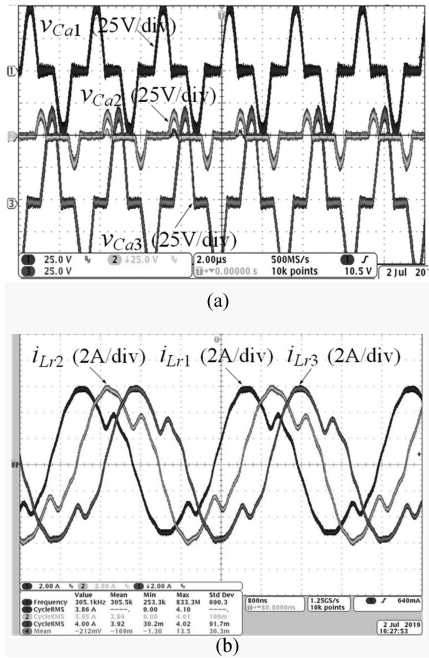


Fig. 17. Waveforms of three-phase circuits operation at 380 V input, 14 V/260 A output. (a) SCC capacitor voltage v_{Ca1} , v_{Ca2} , and v_{Ca3} . (b) Resonant current i_{Lr1} , i_{Lr2} , and i_{Lr3} .

third-phase circuits operate at 250 V input and 14 V output voltage with 100 A load current, switching frequency is 269 kHz and the delay angles α are 148° and 135° , respectively, in the second- and third-phase SCC circuits. Two resonant currents i_{Lr2} and i_{Lr3} are very closely balanced by adjusting the delay angle α in the two SCC circuits.

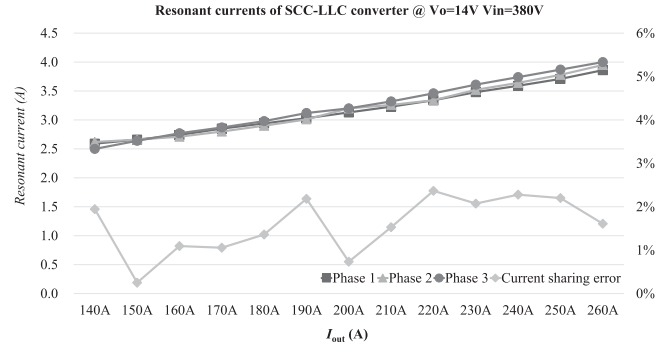


Fig. 18. RMS resonant current i_{Lr1} , i_{Lr2} , and i_{Lr3} at 380 V input 14 V output with three-phase circuits operation.

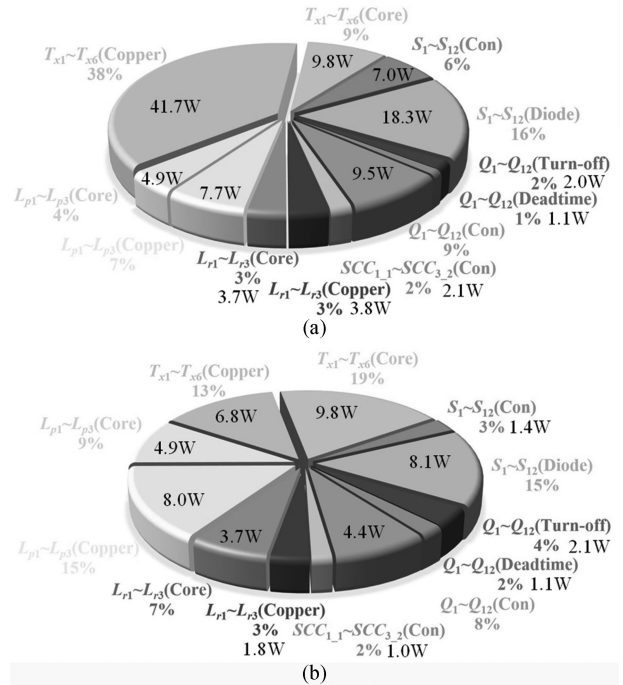


Fig. 19. Loss breakdown of the proposed LDC. (a) Power loss distribution at full load. (b) Power loss distribution at half load.

As shown in Fig. 16, when the three-phase circuits of the proposed LDC operate at 380 V input and 14 V output voltage with 200 A load current, switching frequency is 311 kHz and the delay angles α are 144° , 150° , and 132° , respectively, in the three SCC circuits. Fig. 17 shows the waveforms when input is 380 V and output is 14 V / 260 A with three-phase operation. The switching frequency is 305 kHz and the delay angles α are 136° , 154° , and 126° , respectively, in the three SCC circuits. From Figs. 16 and 17, the resonant currents of the three-phase LLC dc-dc converters are balanced well by adjusting the delay angle α under different operation conditions.

Fig. 18 shows rms resonant current at 380 V input 14 V output with the three-phase circuits operation. When load current increases from 140 to 260 A, the current sharing error $\sigma_{resonant}$ is always smaller than 2.5%, which means three-phase load currents are very balanced.

Power loss breakdown is given in Fig. 19. In this article, the optimal SR conduction time is not concerned as there

TABLE V
COMPARISON BETWEEN THE PROPOSED LDC AND OTHERS LDC

Reference	Specification of the Converter								
	Topology	Configuration	Input voltage	Output voltage	Rated power	Peak efficiency	Full-load efficiency	Rated power density	Switching frequency
[1]	Phase-shift full bridge converter	1 module	200V~400V	12V	1.2kW	95.5%	90%	0.5kW/L	100kHz
[2]	Phase-shift full bridge converter	1 module	300V	12V	2kW	94%	93.2%	-	227kHz~297kHz
[3]	Phase-shift full bridge converter	1 module	235V~431V	11.5V~15V	2kW	93.5%	93%	0.94kW/L	200kHz
[4]	Phase-shift full bridge converter	1 module	300V~400V	12V~16V	0.7kW	93.5%	90%	-	100kHz
[5]	Phase-shift full bridge converter	1 module	250V~400V	13V~15V	1kW	93%	92%	-	100kHz
[6]	Phase-shift full bridge converter	3 modules in parallel	300V	14V	1.2kW	94.7%	93.9%	-	100kHz
[7]	Three-level phase-shift half bridge converter	1 module	200V	12V	0.5kW	91%	90%	-	40kHz
[8]	Two-stage converters	2 modules in parallel	200V~400V	12V	2kW	95.9%	94.3%	-	100kHz~133kHz
[14]	LLC converter	1 module	220V~450V	6.5V~16V	2.5kW	93.2%	92%	1.17kW/L	90kHz~200kHz
[15]	LLC converter	1 module	260V~430V	12.5V~14.5V	1.9kW	93%	91%	1.02kW/L	65kHz~150kHz
[16]	LLC converter	2 modules in parallel	330V~410V	14V	2.5kW	95%	93%	1kW/L	250kHz
[17]	LLC converter	1 module	300V~430V	12V	3kW	94%	93%	21.4kW/L	320kHz~500kHz
[40]	-	-	250V~420V	12V~13.5V	2kW	90%	-	0.26kW/L	-
[41]	-	-	180V~450V	9V~16V	3kW	94%	92%	0.53kW/L	-
[42]	Buck-Boost converter+Series resonant converter	1 module	220V~450V	8V~16V	3.5kW	93.5%	-	1.11kW/L	40kHz~150kHz
[43]	-	-	240V~430V	9V~16V	4kW	93%	92%	0.38kW/L	-
[44]	-	-	250V~425V	13.8V	2.4kW	82%	-	0.6kW/L	-
[45]	Buck converter +LLC DCX	1 module	250V~450V	10V~16V	3.5kW	96%	92%	1.3kW/L	200kHz
[46]	Phase-shift full bridge converter	1 module	200V~310V	12.8V~15.1V	1.8kW	91.9%	90%	8.1kW/L	700kHz
The proposed LDC	SCC-LLC converter	3 modules in parallel	250V~430V	9V~16V	3.8kW	96.7%	95.8%	3kW/L	260kHz~400kHz

are many methods to optimize the SR conduction time [10], [39]. In the proposed LDC, NCP4305 SR chip is used and constant conduction time 0.825 μ s of SR switches is adopted. If SR conduction time is optimized, the body diode loss of S_{1-12} could be removed, and the efficiency can be improved further.

Fig. 20 shows the efficiency of single-phase, two-phase, and three-phase circuits at 380 V input and 14 V output. Phase shedding is used to achieve the highest efficiency for each load range. When the input voltage is 380 V, single-phase circuit operates at from 0 A load current to 80 A load current, two-phase circuits operate from 80 A load current to 130 A load current, and three-phase circuits operate from 130 A load current to 260 A load current.

Fig. 21 shows the efficiency curves of the proposed LDC at different input voltage and 14 V output voltage. In total, 95% and higher efficiency can be achieved over the wide load ranges

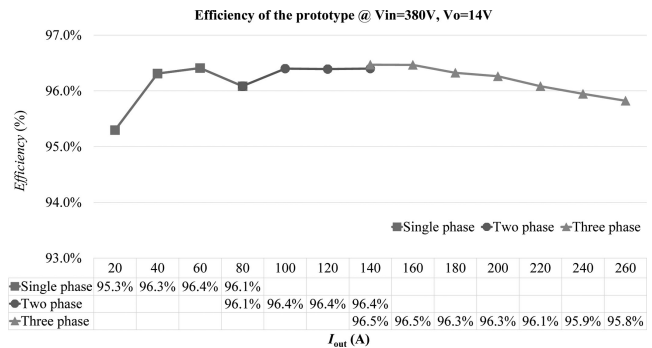


Fig. 20. Efficiency of single-phase, two-phase, and three-phase circuits at 380 V input and 14 V output.

(from 20 A load to full load). When the input voltage is 380 V and output voltage is 14 V, 95.8% efficiency is achieved at 260 A load current, and peak efficiency is 96.7%.

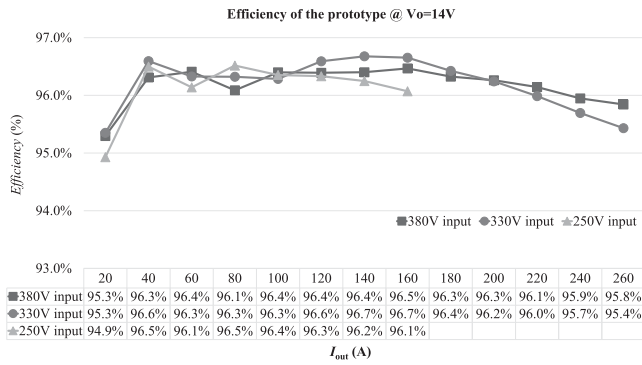


Fig. 21. Efficiency of the proposed LDC when the output voltage is 14 V.

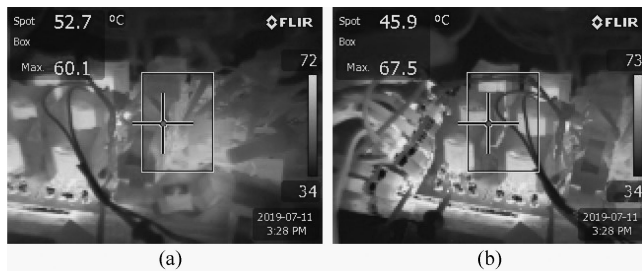


Fig. 22. Thermal images at 380 V input, 14 V/260 A output with 25 °C fluid liquid cooling and fan cooling. (a) Input terminal. (b) Output terminal.

Fig. 22 shows the thermal images at 380 V input, 14 V/260 A output with 25 °C fluid liquid cooling and fan cooling, and the temperature is lower than 80 °C.

The performance of EV LDC as presented in recent literatures [1]–[8], [14]–[17], [45]–[46] and the products [40]–[44] is summarized in Table V for a comprehensive comparison. It shows that with SCC technology, the LDC designed in this article achieves high efficiency and high power-density at the same time.

VII. CONCLUSION

To reduce the conduction loss at high load current, three-phase interleaved LLC dc–dc converters in parallel are designed for EV LDC in this article. SCC circuit is added into resonant tank to achieve current sharing among three phases. In the proposed LDC, GaN HEMTs are used in transformer primary side, allowing the switching frequency to be increased while the volume of the circuit is reduced. ZVS turn-ON of the primary switches and ZCS turn-OFF of secondary SRs are achieved. ZVS operation and low-conduction loss of the SCC circuit switches are also achieved. By adjusting the delay angle α of SCC, three-phase resonant currents are balanced. Two PCB board structure and the liquid cooling cold plate are designed to improve the power density and limit the temperature rise. The proposed LDC achieves an efficiency of 95.8% at 260 A load current and a peak efficiency of 96.7% with a 3 kW/L power density. Phase shedding is used for different load currents, which results in high efficiency over the full load range. Compare with others LDC, the proposed LDC achieves both high efficiency and high power-density simultaneously.

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Xiang Zhou (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2013 and 2018, respectively.

From June 2018 to December 2019, he was with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, as a Postdoctoral Research Fellow. Since 2019, he has been with the Xi'an Jiaotong University, where he is currently an Assistant Professor with the School of Electrical Engineering. His current research interests include soft switching dc–dc converter and dc–ac converter topology and control, resonant converters and server power supplies, and EV chargers.



Bo Sheng (Student Member, IEEE) received the M.S. degree from the Shanghai University of Electric Power, Shanghai, China, in 2016, and the Ph.D. degree from Queen's University, Kingston, ON, Canada, in 2020, both in electrical and computer engineering.

He is currently a Postdoctoral Researcher with Queen's University, Kingston, ON, Canada. His research interests include high-efficiency isolated resonant ac–dc and dc–dc converters, and the corresponding control strategies.



Wenbo Liu (Student Member, IEEE) received the B.Sc. degree from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2014, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2020.

His research interests include topology and control of power converters for electric vehicle (EV) and power delivery (PD), miniaturized resonant converters with wide voltage range and improved thermal performance, and multiphysics, including magnetic and thermal, finite element analysis (FEA) of power magnetic components.



Yang Chen (Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the Beijing Institute of Technology, Beijing, China, in 2011 and 2013, respectively, and the Ph.D. degree in electrical and computer engineering from Queen's University, Kingston, ON, Canada, in 2017.

He has authored more than 30 technical papers published in IEEE journals and conferences. He is the inventor of one China issued patent and six U.S. issued patents with three U.S. patents pending. His research interests include topology and control of

power converters for datacenter and server power supplies, miniaturized resonant converters with wide voltage range for notebook and cellphone fast charging, and high-performance dc–dc converters and ac–dc chargers for EV.

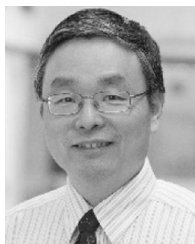


Laili Wang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, in 2004, 2007, and 2011, respectively.

Since 2011, he has been a Postdoctoral Research Fellow with the Electrical Engineering Department, Queen's University, Kingston, ON, Canada. From 2014 to 2017, he was an Electrical Engineer with Sumida, Canada. In 2017, he joined with Xi'an Jiaotong University, as a Full Professor. His research interests include package and integration, wireless

power transfer, and energy harvesting.

Dr. Wang is currently an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is the Vice-Chair of Technical committee of Power Conversion Systems and Components (TC2) in PELS, Co-Chair of System Integration and Application in International Technology Roadmap for Wide Band-gap Power Semiconductor (ITRW), and the Chair of IEEE CPSS&PELS Joint Chapter in Xi'an, China.



Yan-Fei Liu (Fellow, IEEE) received the bachelor's and master's degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1984 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

He was a Technical Advisor with the Advanced Power System Division, Nortel Networks, Ottawa, ON, Canada, from 1994 to 1999. Since 1999, he has been with Queen's University, where he is currently

a Professor with the Department of Electrical and Computer Engineering. His current research interests include optimal application of GaN and SiC devices to achieve small-size and high-efficiency power conversion, 99% efficiency power conversion with extremely high power-density, digital control technologies for high efficiency, fast dynamic response dc-dc switching converter and ac-dc converter with power factor correction, resonant converters and server power supplies, and LED drivers. He has authored around 250 technical papers in the IEEE Transactions and conferences, and holds 35 U.S. patents. He has written a book on *High Frequency MOSFET Gate Drivers: Technologies and Applications*, (IET, 2017). He is also a Principal Contributor for two IEEE standards.

Dr. Liu was the recipient of "Modeling and Control Achievement Award" from the IEEE Power Electronics Society in 2017, Premier's Research Excellence Award in 2000 in Ontario, Canada, and the Award of Excellence in Technology in Nortel in 1997. He was the Vice President of Technical Operations of IEEE Power Electronics Society (PELS, from 2017 to 2020). He has been an Editor of IEEE JOURNAL OF EMERGING AND SELECTED TOPICS OF POWER ELECTRONICS (IEEE JESTPE) since 2013. He was the General Chair of ECCE 2019 held in Baltimore, USA, in 2019. His major service to IEEE is listed as follows: a Guest Editor-in-Chief for the special issue of Power Supply on Chip of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2011 to 2013; a Guest Editor for special issues of JESTPE: Miniaturization of Power Electronics Systems in 2014 and Green Power Supplies in 2016; as Co-General Chair of ECCE 2015 held in Montreal, Canada, in September 2015; the Chair of PELS Technical Committee (TC1) on Control and Modeling Core Technologies from 2013 to 2016; the Chair of PELS Technical Committee (TC2) on Power Conversion Systems and Components from 2009 to 2012.



Paresh C. Sen (Life Fellow, IEEE) was born in Chittagong, Bangladesh. He received the B.Sc. (with hon.) degree in physics and M.Tech. degree in applied physics from the University of Calcutta, West Bengal, India, in 1958 and 1962, respectively, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1965 and 1967, respectively.

He is currently an Emeritus Professor of Electrical and Computer Engineering with Queen's University, Kingston, ON, Canada. He has worked for industries

in India and Canada and was a Consultant to electrical industries in Canada. He has authored more than 215 technical papers in the general area of electric motor drives and power electronics. He is the author of two internationally acclaimed textbooks: *Principles of Electric Machines and Power Electronics* (Wiley 1989, 1997, 2013) and *Thyristor DC Drives* (Wiley, 1981). He has taught electric machines, power electronics, and electric drive systems for over 45 years. His fields of interest include power electronics, electric drive systems, switching power supplies, wind energy systems, digital control, and modern control techniques for power electronics, and motor drive systems.

Dr. Sen has served IEEE in various capacities: as an Associate Editor, Distinguished Lecturer, Chairman of the technical committees on power electronics and energy systems, Session Organizer, Session Chairperson, and Paper Reviewer. He was an Natural Science and Engineering Research Council of Canada (NSERC) Scientific Liaison Officer evaluating university-industry coordinated projects. He is globally recognized as an authority in power electronics and motor drive systems. He was the recipient of the IEEE-IAS (Industry Application Society) Outstanding Achievement Award in 2008, and the IEEE-Canada Outstanding Engineering Educator Award in 2006 for his Outstanding Contributions over four decades as a Researcher, Supervisor, Teacher, Author, and Consultant, the IAS-IDC Prize Paper Award in 1986. He is a fellow of EIC. As an Emeritus Professor, he continues to be active in research, supervision of graduate students and in several IEEE societies.