Zero Inductor-Voltage Multilevel Bus Converter

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***Abstract*—A novel topology to achieve 4:1 voltage step down, aimed at 48 V to 12 V conversion in data center applications, is presented. The so-called dc-transformer topologies have become a very active area of research to improve the overall efficiency of data centers in response to a shift from a 12 Vdc bus architecture to a 48 Vdc bus architecture. In particular, switched-capacitor topologies have been investigated due to their high power density, efficiency, and low reliance on magnetics. However, switched-capacitor topologies have challenges associated with the hard-charging of capacitors and are often forced to make design compromises that reduce their overall performance. The proposed topology maintains many of the advantages of a switched capacitor topology, such as reduced component stresses, and very low reliance on magnetics, while also inherently avoiding any hard-charging of the flying capacitors. This allows the converter to operate at a very low frequency, such as 60 kHz, with a small inductor, such as 100 nH, and use low voltage stress devices to achieve a peak efficiency of more than 99% for 48 V to 12 V conversion and a power density of 800 W/in^3.**

***Index Terms*—48 V to 12 V, bus converter, data center, dc–dc converter, dc-transformer (DCX), high efficiency, intermediate bus.**

I. Introduction

DATA centers and servers are one of the largest growing consumers of electrical power in the world today. The Information and Communication Technology (ICT) sector consumes approximately 7% of the world's electricity, and this number is projected to rise to 13% by 2030 [1]. With advances in cloud computing and the massive expansion in the use of Internet services worldwide, data centers are expected to be one of the fastest-growing consumers of electricity within the ICT sector, increasing by up to 20% per year [2]. In 2017, there were 8.4 billion "Internet of Things" connected devices. This is expected to rise to over 20 billion devices by 2020, as over 1 billion new Internet users are expected to emerge during that time, growing from 3 billion to over 4 billion [3].

Data center architecture has evolved over time and significant gains have been realized at the building level power conversion steps; however, as given in Table I, the majority of the loss still occurs at the server power supply unit (PSU) and board-level voltage regulators [4], [5]. Google's approach has been to implement what they refer to as a 48 V power architecture [6].

TABLE I
Efficiency Breakdown of Server Power Supplies [4], [5]

UPS	PDU	Rack-Level Converter	**Server PSU**	**VR Stage**	Overall
Traditional AC					
89.2%	93.2%	N/A	**75.5%**	**81.6%**	51.6%
High-Efficiency AC					
97.1%	94.0%	N/A	**88.0%**	**87.7%**	69.9%
Rack-Level 48VDC					
97.1%	93.8%	92.38%	**91.5%**	**87.7%**	67.4%
Facility-Level 400VDC					
95.3%	96.8%	N/A	**89.1%**	**87.7%**	72.7%

In this architecture, the server PSU distributes 48 V throughout the server rack, which is then converted to the voltage required at the point of load. Google has estimated that this change can reduce their conversion losses by 30%, as well as offering a 16× reduction in the distribution losses throughout the rack [7]. Overall, this has the potential to greatly reduce cost and improve both efficiency and flexibility. However, this 48 V to POL conversion can be very challenging, particularly for low-voltage high-current loads, such as modern processors or graphics cards. With next-generation processors consuming even larger amounts of power to support higher speeds, this challenge is only going to grow. The most common approach to handle this extremely high-current demand is to utilize a "two-stage" conversion approach, such as the intermediate bus architecture, to achieve this stepdown at high efficiency [8]–[12].

Research into new topologies suited for this intermediate bus converter application has become a very active area, with many different topologies being proposed. In particular, switched-capacitor converters (SCC) are being investigated due to their very high power density and efficiency. In an intermediate bus converter application, the bus converter can be operated as a "dc-transformer" (DCX) where output voltage regulation is not required, and one of the main disadvantages of SCC, namely the inability to achieve lossless regulation, can be avoided [13]. The work presented in this article is an improvement on the zero-inductor voltage converter topology first presented at APEC 2018 [14]. Section II will discuss some of the existing SCC topologies being investigated, as well as the key drawbacks of these technologies. Section III will present the zero-inductor voltage converter and discuss the key operating principles of this novel topology. Section IV will present a detailed analysis of the circuit topology and design considerations. Section V will present the loss analysis and simulation waveforms. Section VI

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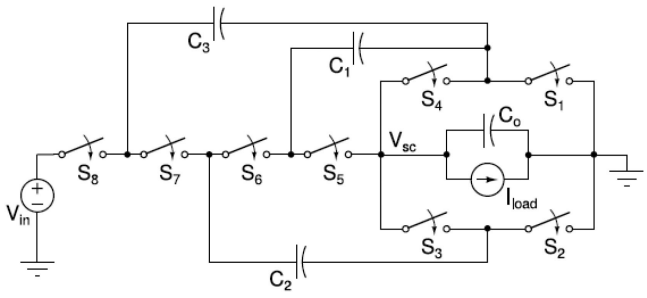

Fig. 1. Dickson SCC topology, referenced from [17].

will present the experimental results, and Section VII will conclude this article.

II. Overview of Capacitor-Based Converters for Intermediate Bus Applications

In many SCC topologies, it is not possible, or at least not easy, to achieve lossless regulation of the output voltage. Typically, in an SCC topology, the optimal operating point will occur at some integer-ratio step-down, 4:1 step-down, for example. In many applications, this is undesirable; however, in an intermediate bus architecture, the intermediate bus converter can operate as a DCX or dc-transformer, and output voltage regulation is not required. As a result of this, SCC have become widely researched for these DCX applications in data centers. Additionally, in most conventional dc–dc converters, the magnetic components are the largest components and are lossy. SCC aim to remove, or at least significantly reduce, the need for any magnetic components in the converter to achieve much higher power densities and efficiencies than conventional topologies [15].

A. Conventional Dickson SCC

One of the most widely studied SCC topologies is the Dickson SCC topology [16]. In particular, the Dickson converter offers extremely good utilization of the semiconductor devices. The voltage stress of each MOSFET will be reduced to either 0.5 V_{in} or 0.25 V_{in} due to the flying capacitors used in the topology. As there are multiple capacitor branches supplying the output current in parallel, the rms current of the MOSFETs and capacitors is significantly reduced, making the Dickson converter very attractive for high-current applications where the conduction loss becomes dominant.

However, the Dickson converter, like most conventional SCC topologies, suffers from a significant drawback associated with the hard-charging of the capacitors [17]. The key operating principle behind most SCC topologies, including the Dickson converter, is that the capacitors are connected in series during certain switching states, and in other switching states are connected in parallel. The 4:1 Dickson converter is shown in Fig. 1.

The switches are driven in such a way that this circuit has two states, shown in Fig. 2. In these switching states, the capacitor branches are connected in parallel, with each carrying part of the load current. This is one of the key advantages of the Dickson converter, as by sharing the current between multiple paths, the

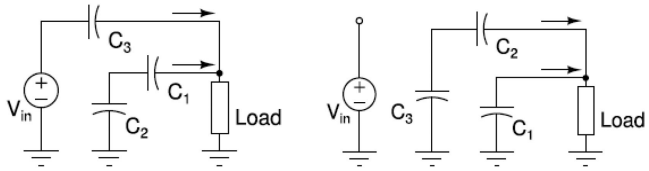

Fig. 2. Dickson converter switching states, referenced from [17].

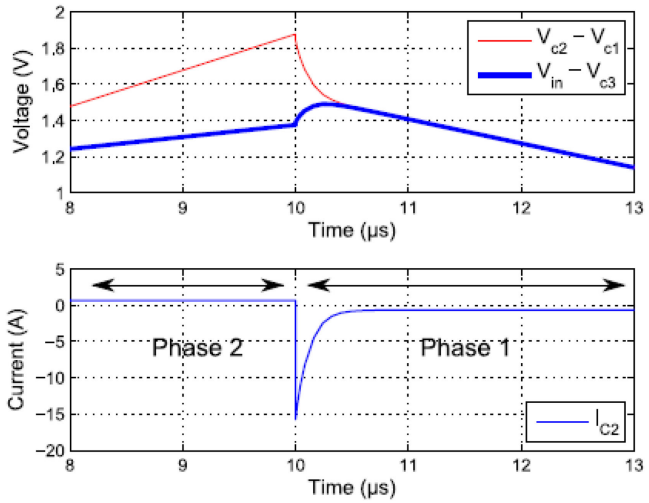

Fig. 3. Dickson SCC example capacitor current spike, caused by parallel connection of mismatched flying capacitors, referenced from [17].

overall conduction loss is reduced. However, this paralleling of capacitors also has a major drawback. During normal operation, the capacitor ripple voltages on these capacitors will diverge, meaning that at the time of switching, there will always be some voltage mismatch between the paralleled flying capacitors as shown in Fig. 3. This voltage mismatch will be applied across a very low impedance connection through the ON-state switches resulting in a significant current spike as the branch voltages equalize. It is this parallel connection of capacitors that causes a serious issue for the Dickson converter and many other SCC topologies.

The resulting current spike can increase the loss of the converter substantially, and therefore, the SCC must be carefully designed to minimize these current spikes. However, significant design tradeoffs are required. At the heart of the challenge is minimizing the voltage difference between the capacitors when they are connected in parallel, which requires the capacitor ripple voltage to be reduced. Typically, this can only be achieved by increasing the switching frequency or increasing the value of the capacitors. Increasing the switching frequency results in higher switching losses, while increasing the value of the capacitors reduces the power density.

An example of a 48 V to 12 V Dickson SCC is presented in [18]. For a single-phase converter, the maximum output power of the prototype was 480 W (12 V 40 A output). The converter achieved a peak efficiency of 98%, with a full load efficiency of approximately 96.5%, and a power density of 400 W/in^3. This a much lower efficiency and power density than results that have

been achieved by other, more conventional, topologies, such as an *LLC* DCX [19].

The reduced power density and efficiency in the conventional Dickson SCC are primarily due to the hard-charging of capacitors. In order to mitigate the impact of the current spikes, the Dickson SCC design used extremely large capacitors of up to 500 and 400 μF, while also using a switching frequency of 200 kHz. Due to these design compromises, the theoretical advantage of switched-capacitor topologies over traditional topologies is reduced, if not eliminated completely. Therefore, techniques to "soft-charge" the capacitors in SCC topologies have received a lot of attention.

B. SCC With Current Limiting Inductor

One technique that can be used to limit the current spike through the capacitors during switching transitions is to include an inductor in the SCC topology [20]–[22]. As the inductor will be in the current branch, the current spike at the time of switching can be limited, even if only a relatively small inductor is used. However, in many topologies, such as the Dickson converter, one single inductor is not enough to achieve full soft-charging. Using the example of a Dickson converter, if an inductor is placed at the output to form an *LC* output filter, this will eliminate the charging spike associated with the output capacitor, but it will not avoid the charging spike between the paralleled current branches in the circuit. This means that for a Dickson converter, more than one inductor would be required to achieve full soft-charging. Examples do exist of utilizing a Dickson SCC topology with two or more inductors added to achieve full soft-charging, such as Google's proposed switched-tank converter [23], [24].

Adding these inductors to SCC can allow them to achieve soft-charging, however once again this causes a tradeoff in the practical design where efficiency and power density must be sacrificed to achieve this improvement in performance. Requiring multiple inductors, in essence, defeats the original purpose of the SCC, which is to minimize the reliance on magnetic components. While these inductors can be small, they often are also used as part of a resonant tank circuit to achieve soft-switching and further reduce the loss of the converter. These resonant converters are often sensitive to component tolerances, which can be quite large for capacitive and inductive elements, and present a challenge when scaling to higher power levels through techniques such as paralleling multiple phases.

C. Split-Phase Dickson SCC Converter

In some SCC topologies, it may be possible to achieve soft-charging through a modification of the control scheme, avoiding some of the critical downsides associated with adding components to the circuit topology. An example of this is the split-phase control technique for the Dickson SCC [16] as shown in Fig. 4. In the split-phase control technique of the Dickson converter, additional operating states are added where only one capacitor branch is supplying the load current. By introducing these states, it is possible to ensure that the voltages of the capacitor branches are matched at the time of switching as shown in Fig. 5.

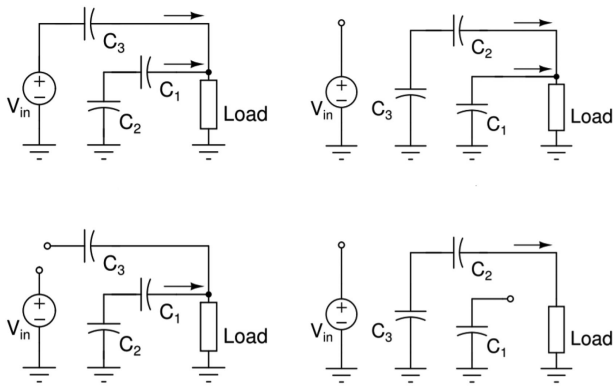

Fig. 4. Split-phase control scheme for 4:1 Dickson converter, referenced from [17].

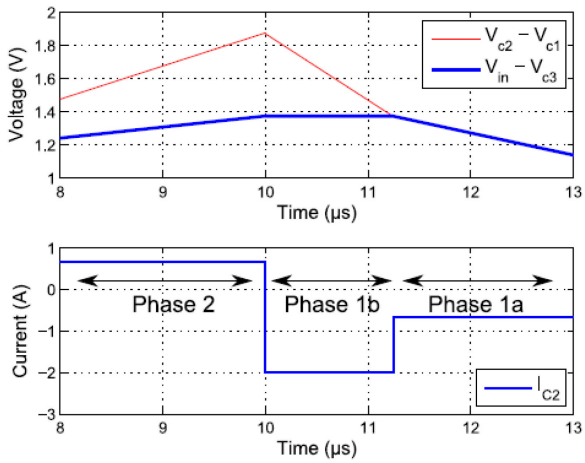

Fig. 5. Split-phase control scheme for 4:1 Dickson converter, referenced from [17].

In theory, this technique can completely eliminate the hard-charging current spike. However, to achieve this in a practical circuit, there are additional factors that must be considered. In the split-phase control, either additional control circuitry is needed to sense the capacitor voltages and perform switching at the correct time or the capacitor values in the circuit must be exactly matched. This is a significant challenge in the split-phase Dickson SCC as all three capacitors have different voltage ratings, meaning that the dc-derating of ceramic capacitors will significantly impact the "real" capacitance value in the circuit.

Additionally, capacitors often have a relatively large component to component variations of up to 20% as making exact matching in a production design is very difficult. This means that while the control strategy can mitigate the effect of the hard-charging current spikes, it cannot eliminate them entirely in a practical circuit design. Additionally, by introducing states where the current is carried by only one branch, the conduction loss of the split-phase Dickson SCC is increased when compared with an "ideal" Dickson SCC operating using conventional control. This conduction loss increase can be up to 20% or 30% for high-current loads where the conduction loss is dominating the overall efficiency of the converter.

A key takeaway here is that regardless of the SCC topology chosen and regardless of the technique used to try to achieve soft-charging, there is always a design tradeoff that compromises performance in one of the key metrics, namely efficiency and power density.

D. Multilevel Modular Capacitor-Clamped Converter (MMCCC)

The MMCCC is a multilevel capacitor-based converter topology that offers promising performance for utilization in high-power dc–dc converter applications, particularly for hybrid electric vehicle applications where its bidirectional power handling capability can be utilized [25]. The MMCCC offers a modular design and greatly simplified switching scheme when compared with many other flying capacitor multilevel dc converters. Due to the multilevel structure, the voltage stress of the individual MOSFETs will be reduced, and the bulky magnetic components used in conventional topologies can be eliminated. The MMCCC, however, suffers from many of the same drawbacks as the SCC topologies previously discussed. As the capacitor branches in the circuit will be connected in parallel through the low-impedance switches, this will result in current spikes and charge redistribution loss similar to an SCC topology. This loss must be mitigated through the combined use of large flying capacitors and higher switching frequencies, which increase the size of the converter and reduce the efficiency.

Similar to the SCC topologies, it is possible to achieve resonant operation with the MMCCC. A technique has been proposed to achieve zero current switchings for the MMCCC by utilizing additional inductance in the circuit [26]. While this technique does help to reduce the switching losses by achieving zero current switchings and reducing the required capacitor size for the converter, it adds significant design complexity and the parasitic inductance of the converter may not be sufficient for an optimal resonant design. In the optimal design presented in [26], there are four "stray" inductances added to the circuit with values of 250 nH for L_{s1} and 500 nH for $L_{s2\text{-}4}$. This substantial amount of added inductance contributes to a large increase in the conduction loss for the topology while also increasing the size. The complexity of this resonant design may also present a challenge for a mass-produced design in a data center application. Another critical drawback of the MMCCC design is the large number of components required. For a 4:1 step-down ratio, the MMCCC requires three flying capacitors and ten switches. This high component count will increase the size of the converter and having a larger number of components in the conduction path will increase the conduction losses of the converter. At the high-current levels demanded in data center applications, minimizing the conduction loss becomes one of the primary design criteria.

III. Zero Inductor-Voltage (ZIV) Converter Topology and Operating Principles

The technical approach used in this article is different from the above-mentioned MMCCC or SCC converter using an inductor as a current limiting component. It is proposed in this article that a pulsewidth modulation (PWM) switching converter can include an inductor, operate at PWM mode, and operate in such a way that there is zero voltage across the inductor. More specifically, the voltage across the inductor is independent of the input and output voltages and will instead be the ripple voltage of the input capacitor, output capacitor, and flying capacitor, which are much smaller than the input and output dc voltages. The capacitors in this topology are always connected in series not in parallel. The voltage stress of the MOSFETs is also reduced by the flying capacitors. Since it is derived from a PWM converter, the operation of the converter is not sensitive to the capacitor or inductor value tolerance. As a result, the design of this converter is greatly simplified.

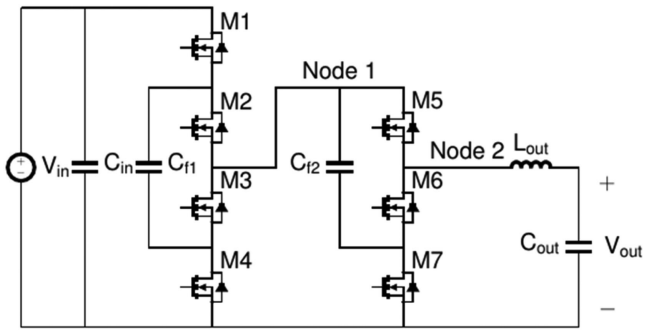

Fig. 6. Seven-switch ZIV converter topology.

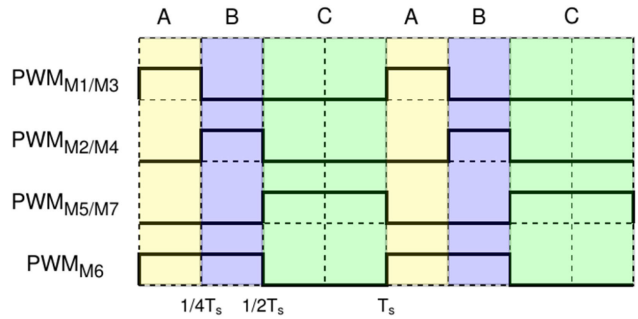

Fig. 7. Seven-switch ZIV converter PWM gate signal diagram.

A. Proposed Seven-Switch ZIV Converter

The ZIV converter utilizes seven MOSFETs and two flying capacitors in the topology shown in Fig. 6. The PWM gate drive signals are shown in Fig. 7. From this, it can be observed that the converter has three switching states, labeled A, B, and C. The equivalent circuit for each switching state is shown in Fig. 8. In switching state A, MOSFETs M1, M3, and M6 are turned ON. Both flying capacitors are being charged in this state, for the first 25% of the switching period. In switching state B, MOSFETs M1 and M3 are turned OFF, M2 and M4 are turned ON, and M6 remains ON. The first flying capacitor C_{f1} is now being discharged, while C_{f2} continues to charge, for the next 25% of the switching period.

In switching state C, all the first-stage MOSFETs (M1–M4) are now turned OFF. MOSFET M6 is turned OFF, and MOSFETs M5 and M7 are turned ON. C_{f1} is now disconnected and does not carry

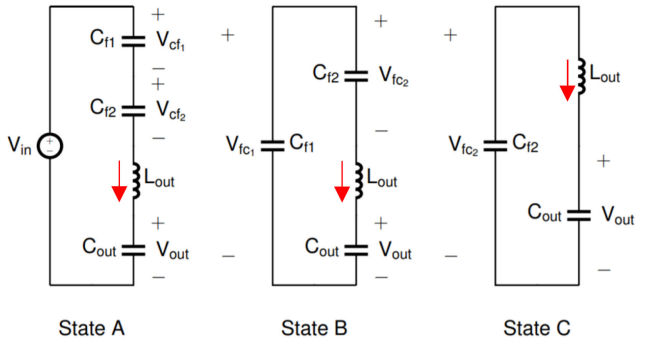

Fig. 8. Equivalent circuits in switching states A, B, and C.

any current during this switching state, while C_{f2} is discharged for the remaining 50% of the switching period.

As can be seen from these figures, the flying capacitors are never placed in parallel, and the inductor is always in the current path. This means that there is no current spike through the capacitors; soft-charging is an inherent trait of the topology and does not depend on any particular component tolerances or additional inductors added to the current-carrying branches.

B. Steady-State Operation

In order to understand the 4:1 step-down ratio provided by this converter topology, the inductor voltage can be analyzed in the steady state where V_{LA} is the inductor voltage in State A, V_{LB} is the inductor voltage in State B, V_{LC} is the inductor voltage in State C, $V_{Cf1\text{-}A}$ and $V_{\mathrm{Cf2\text{-}A}}$ are the two flying capacitor voltages in State A, $V_{\mathrm{Cf1\text{-}B}}$ and $V_{\mathrm{Cf2\text{-}B}}$ are the two flying capacitor voltages in State B, and $V_{\mathrm{Cf2\text{-}C}}$ is the second flying capacitor voltage in State C

$$V_{LA} = V_{\mathrm{in}} - V_{cf1-A} - V_{cf2-A} - V_{\mathrm{out}} \text{ State A} \quad (1)$$

$$V_{LB} = V_{cf1-B} - V_{cf2-B} - V_{\mathrm{out}} \text{ State B} \quad (2)$$

$$V_{LC} = V_{cf2-C} - V_{\mathrm{out}} \text{ State C.} \quad (3)$$

As seen from the gate signal diagram (see Fig. 7), State A is active for 25% of one switching cycle, State B is active for 25% of one switching cycle, and State C is active for the remaining 50% of the switching cycle. Thus, the average inductor voltage over one switching cycle can be expressed as

$$V_L = \frac{V_{LA}}{4} + \frac{V_{LB}}{4} + \frac{V_{LC}}{2}. \quad (4)$$

Note that the capacitor balance must also be maintained for steady-state operation. This means that the average voltage of C_{f1} in State A must be equal to the average voltage of C_{f1} for State B, as C_{f1} is charged for 25% of the switching cycle in State A, discharged for 25% of the switching cycle in State B, and is disconnected in State C

$$V_{cf1-A} = V_{cf1-B}. \quad (5)$$

For C_{f2}, the average voltage of C_{f2} across both States A and B must be equal to the average voltage of C_{f2} across State C. This is because C_{f2} is charged for 25% of the switching cycle in State A, continues to be charged for 25% of switching cycle in State B, and then is discharged for the remaining 50% of the switching cycle in State C

$$\frac{V_{cf2-A} + V_{cf2-B}}{2} = V_{cf2-C}. \quad (6)$$

Substituting (1)–(3) into (4) gives the expanded form

$$V_L = \frac{V_{\mathrm{in}}}{4} - \left(\frac{V_{cf1-A}}{4} - \frac{V_{cf1-B}}{4}\right) - \left(\frac{V_{cf2-A}}{4} + \frac{V_{cf2-B}}{4} - \frac{V_{cf2-C}}{2}\right) - V_{\mathrm{out}} \quad (7)$$

$$V_L = \frac{V_{\mathrm{in}}}{4} - (0) - (0) - V_{\mathrm{out}} = 0. \quad (8)$$

Under steady-state operation, the average inductor voltage across one switching cycle must be zero, and utilizing the equivalencies given in (5) and (6), the capacitor voltage terms cancel out as shown in (8) leaving

$$V_{\mathrm{out}} = \frac{V_{\mathrm{in}}}{4}. \quad (9)$$

Thus, the seven-switch ZIV converter provides a fixed 4:1 step-down ratio under steady-state operation.

IV. ZIV Converter Detailed Analysis

The ZIV converter has two key features that enable it to achieve extremely high performance. The first is the multilevel structure that reduces the voltage stress of the MOSFETs and flying capacitors. The second is the ZIV property for which the converter is named. This property means that the output inductor sees only the small capacitor ripple voltage, which is independent of the dc voltage value, and thus, a very small inductance value can be utilized.

A. Capacitor Balancing

The multilevel structure is a key advantage of the ZIV converter topology enabling a reduction in the component voltage stress. For the input-stage, consisting of M1–M4, the flying capacitor is nominally charged to 0.5 V_{in}, as shown later in this section. This means that the maximum voltage stress of each MOSFET in the input stage is also reduced to 0.5 V_{in}, neglecting the capacitor ripple. In the second stage, the capacitor is nominally charged to 0.25 V_{in}, reducing the voltage stress of each output stage MOSFET to a maximum of 0.25 V_{in}. As the voltage stress of the devices is dependant on the capacitor voltages, this naturally raises a concern about the capacitor balancing. However, the ZIV converter is self-balancing, with the converter operation naturally ensuring that the capacitors will operate at, or very close to, their nominal value. This can be explained by examining the circuit in Fig. 9.

This circuit represents one of the four switch "building blocks" that make up the converter. Note that in the output stage, the top MOSFET is not needed, as during State C, the input stage MOSFETs are all turned OFF. If we neglect the capacitor ripple, then the steady-state voltage for the capacitor can be found as follows. It is noted that M1 and M3 are ON for 25% of the switching period, and M2 and M4 are ON for the next 25% of

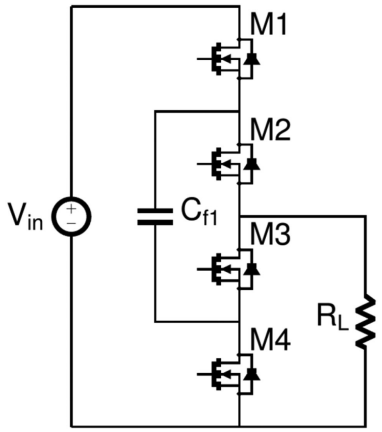

Fig. 9. ZIV Converter first-stage "building-block" circuit.

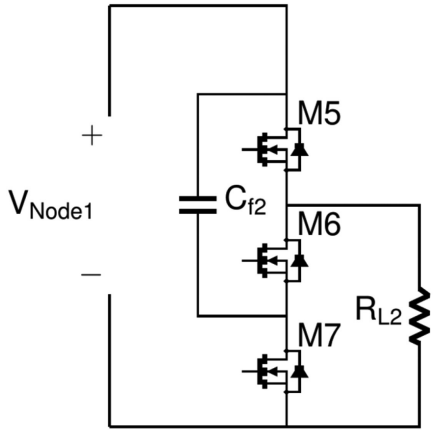

Fig. 10. ZIV converter second-stage "building-block" circuit.

the switching period. These four switches are all OFF for the remaining 50% of the switching period in State C.

$$I_{cf1\_\text{charge}} = \frac{V_{\text{in}} - V_{cf1}}{R_L} \tag{10}$$

$$I_{cf1\_\text{discharge}} = \frac{-V_{cf1}}{R_L}. \tag{11}$$

Then by noting that for steady state, the average current through the capacitor for one switching cycle must be zero

$$I_{cf1} = I_{cf1\_\text{charge}}\ (0.25) + I_{cf1\_\text{discharge}}\ (0.25) = 0 \tag{12}$$

$$0.25\ (V_{\text{in}} - V_{\text{cap}}) = 0.25\,(V_{\text{cap}}) \tag{13}$$

$$V_{\text{cap}} = 0.5V_{\text{in}}. \tag{14}$$

What is important to note here is that the capacitor voltage does not "run away" to V_{in} or zero, it is determined by the 25% duty cycle. Therefore, there is no need for active balancing as, in practice, any mismatch in duty cycles should be small, and therefore, the capacitor voltage will be very close to the expected value, with the impact of the duty cycle or small balance mismatches having far less impact than, for example, the capacitor ripple under heavy load. In the seven-switch ZIV converter case, the duty cycle is always 25%, which means the first flying capacitor voltage will naturally balance to 0.5 V_{in}.

The second flying capacitor C_{f2} is similarly self-balancing. Note that when V_{Cf1} is equal to 0.5 V_{in}, the Node 1 voltage for both States A and B will be equal to 0.5 V_{in} (neglecting capacitor voltage ripple). Thus, the "input voltage" from the perspective of the second stage is always 0.5 V_{in}. A similar "building block" shown in Fig. 10 can be utilized to analyze the second stage. Note that the top MOSFET (M1 in Fig. 9) is removed in the second stage, as during State C (when C_{f2} is discharging), all of the first-stage MOSFETs are turned OFF.

When these first-stage MOSFETs are turned OFF, the Node 1 voltage can be allowed to be pulled down to the C_{f2} voltage

$$I_{cf2\_\text{charge}} = \frac{0.5V_{\text{in}} - V_{\text{cap}}}{R_{L2}} \tag{15}$$

$$I_{cf2\_\text{discharge}} = \frac{-V_{\text{cap}}}{R_{L2}}. \tag{16}$$

Then by noting that for steady state, the average current through the capacitor for one switching cycle must be zero

$$I_{cf2} = I_{-cf2\_\text{charge}}\ (0.5) + I_{cf2\_\text{discharge}}\ (0.5) = 0 \tag{17}$$

$$0.5\ (0.5V_{\text{in}} - V_{\text{cap}}) = (0.5)\ (V_{\text{cap}}) \tag{18}$$

$$V_{\text{cap}} = 0.25V_{\text{in}}. \tag{19}$$

Thus, when the duty cycle of the second stage is 50%, the second-stage flying capacitor will balance to 0.25 V_{in}. This capacitor self-balancing result will also be validated through simulation and experimentally in Sections IV and V.

B. ZIV Property

A second key advantage of this topology, the ZIV operation for which it is named, can be seen by examining the voltage at Node 2 (see Fig. 6). Recall that the first flying capacitor is charged to half of the input voltage nominally, and the second flying capacitor is charged to one-quarter of the input voltage nominally. These capacitor voltages can be expressed as a nominal dc value, summed with a ripple voltage

$$V_{Cf1} = \frac{V_{\text{in}}}{2} + v_{Cf1\text{rip}} \tag{20}$$

$$V_{Cf2} = \frac{V_{\text{in}}}{4} + v_{Cf2\text{rip}}. \tag{21}$$

For State A

$$v_{n2} = V_{\text{in}} - v_{cf1} - v_{cf2} \tag{22.1}$$

$$v_{n2} = V_{\text{in}} - \frac{V_{\text{in}}}{2} - \frac{V_{\text{in}}}{4} - v_{cf1\text{rip}} - v_{cf2\text{rip}} \tag{22.2}$$

$$v_{n2} = \frac{V_{\text{in}}}{4} - v_{cf1\text{rip}} - v_{cf2\text{rip}}. \tag{22.3}$$

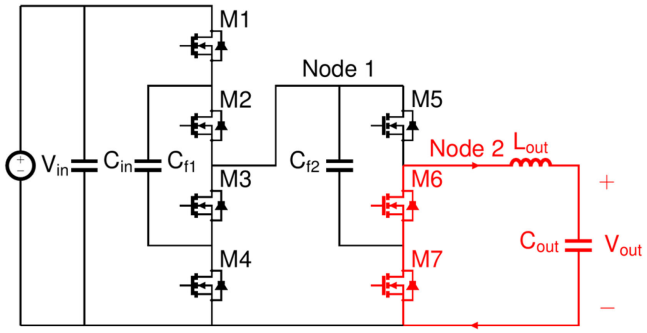

Fig. 11. Deadtime ZIV converter conduction path.

For State B

$$v_{n2} = v_{cf1} - v_{cf2} \tag{23.1}$$

$$v_{n2} = \frac{V_{\text{in}}}{2} - \frac{V_{\text{in}}}{4} + v_{cf1\text{rip}} - v_{cf2\text{rip}} \tag{23.2}$$

$$v_{n2} = \frac{V_{\text{in}}}{4} + v_{cf1\text{rip}} - v_{cf2\text{rip}}. \tag{23.3}$$

For State C

$$v_{n2} = v_{cf2} \tag{24.1}$$

$$v_{n2} = \frac{V_{\text{in}}}{4} + v_{cf2\text{rip}}. \tag{24.2}$$

For all of the above states, the voltage at Node 2 is equal to 0.25 V_{in} plus the capacitor ripple voltage. The inductor is connected between Node 2 and the output voltage, which is also shown to be equal to 0.25 V_{in}. Thus, the only voltage seen by the inductor will be due to the capacitor ripple. This means the inductor voltage is independent of the input and output voltage level. The low voltage stress means that very small inductors, as small as 100 nH, can be utilized even with switching frequencies below 100 kHz.

In addition to the three switching states previously discussed, in the practical circuit deadtime is required to ensure that there is no shoot-through during the switching of the MOSFETs. This results in the introduction of a fourth state, as shown in Fig. 11 . During this time, the inductor current freewheels through the body diodes of M6 and/or M7. Note that during the transition between State A and State B, M6 will remain ON; thus, only M7 will conduct through its body diode for this time. During the deadtime, the voltage at Node 2 becomes equal to the diode drop of the reverse conducting MOSFET's. This will reduce the output voltage and increase the inductor current ripple. However, in a well-designed circuit, this deadtime can be very short, on the order of tens of nanoseconds, and the resulting impact on overall performance is nearly negligible as it is desirable to operate the ZIV converter at relatively low switching frequencies of 100 kHz and below.

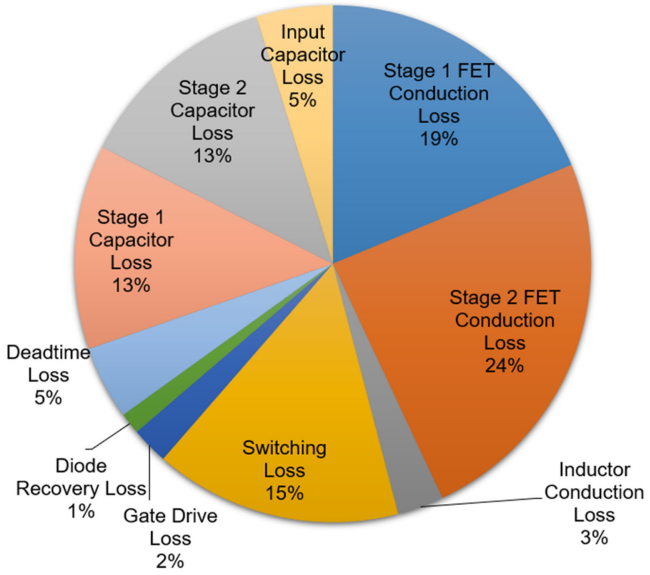

Fig. 12. Loss estimation for 48 V input, 12 V/25 A output, 60 kHz switching frequency.

C. Flying Capacitor Sizing

As the ZIV converter does not rely on resonant operation, it is not sensitive to component tolerances and offers a high degree of flexibility in terms of component selection. One design parameter of note is the sizing of the flying capacitors. The capacitors must be selected such that the voltage ripple of the capacitor does not result in any of the MOSFETs seeing a voltage that exceeds the maximum rating of the device. As the capacitor ripple is proportional to the load current, this calculation should be done under the maximum load current condition $I_{\max}$. If $V_{\text{DS}}(\max)$ is the maximum rating for the MOSFET, V_{cap} is the nominal voltage of the capacitor (either 0.5 V_{in} for C_{f1} or 0.25 V_{in} for C_{f2}) and t_c is the charging time of the capacitor (equal to one-quarter of the switching period for C_{f1} and one half of the switching period for C_{f2}), then the minimum capacitor value for the ZIV converter is given by

$$C > \frac{I_{\max} t_c}{V_{\text{DS(max)}} - V_{\text{cap}}}. \tag{25}$$

An example calculation is provided utilizing 48 V input, 35 A maximum output load, 60 kHz switching frequency, 30-V-rated MOSFETs in the first stage, and 25-V-rated MOSFETs in the second stage

$$C_{f1} > \frac{35\,(0.25\ x\ 16.67\,\mu\text{s})}{30-24} = 24.3\,\mu\text{F} \tag{26}$$

$$C_{f2} > \frac{35\,(0.5\ x\ 16.67\,\mu\text{s})}{25-12} = 22.4\,\mu\text{F}. \tag{27}$$

Note that this is the minimum capacitor value required to avoid damaging the MOSFETs. In the practical design of a ZIV converter, the capacitor ESR is a significant source of loss, and therefore, in order to optimize the efficiency of the converter, it is desirable to use several capacitors in parallel to reduce the ESR.

Ceramic capacitors can be used due to their high capacitance, small size, and low ESR. However, ceramic capacitors have a large derating under a large dc voltage (this derating may be up to 80% depending on the voltage rating and the size of the capacitor) as well as high variation in capacitance value between components (up to 20%). Therefore, in the practical case, the capacitor banks should be designed to be larger to minimize the ESR as well as to provide immunity to the nonideality of ceramic capacitors. This also presents somewhat a tradeoff between efficiency and power density in the ZIV converter design. Larger capacitor banks, with lower ESR, will offer improved efficiency at the cost of overall size. So long as the capacitor meets the minimum value to ensure the MOSFETs are not damaged, an increase in capacitor voltage ripple or inductor current ripple will not substantially affect the operation of the circuit. Therefore, designers have a high degree of flexibility to improve efficiency or reduce the size, depending on their application that would not be possible using a more complex resonant design.

D. Output Inductor Sizing

As with the flying capacitors, the output inductor selection for the ZIV converter is flexible as the inductance value is not dictated by a requirement for resonant operation. The output inductor should be selected based on the output ripple current requirement. It should also be noted that higher output current ripple will increase the ESR loss of the output capacitor, and therefore, similar to the flying capacitor selection in a practical design, it is desirable to use an inductor that may have a higher value than the minimum theoretically calculated value in order to reduce the overall converter loss. The voltage across the inductor will be based on the capacitor ripple voltages, per (22.3), (23.3), and (24.2). Increasing the capacitor size can, therefore, also reduce the inductor ripple current. As shown by the simulation and experimental results, the maximum inductor ripple will generally be dominated by State C, as this state lasts twice as long as State A or B. During State C, the inductor sees only the second flying capacitor ripple, which will be a triangular waveform. Let $A_{cf2\text{-ripple}}$ be the amplitude of the second flying capacitor ripple

$$\Delta\, i_L = \frac{T_s}{4}\,\frac{A_{cf2-\text{ripple}}}{\sqrt{3}L}. \tag{28}$$

As an example calculation, using the simulation parameters presented in Section V

$$\Delta\, i_L = \frac{16.67\,\mu\text{s}}{4}\;\frac{0.68\,\text{V}}{\sqrt{3}\,230\,\text{nH}} = 7.1\,\text{A}. \tag{29}$$

This closely matches the maximum peak-to-peak ripple in the simulated inductor current waveform of 6.8 A. During the deadtime, the Node 2 voltage will be equal to some small negative voltage as the MOSFETs reverse conduct through their body diodes. Therefore, during the deadtime, the inductor will see a negative voltage across its terminals equal to the output voltage plus the reverse voltage of the two MOSFET body diodes. To approximate the impact of this on the overall current ripple, the ripple caused by the deadtime can be added to the peak-to-peak ripple estimated by neglecting deadtime

$$\Delta\, i_{L(\text{deadtime})} = T_{\text{deadtime}}\,\frac{V_{\text{out}} + 2V_{\text{SD}}}{L}. \tag{30}$$

As an example calculation, using the same parameters as the previous calculation, with a deadtime of 5 ns

$$\Delta\, i_{L(\text{deadtime})} = 5\,\text{ns}\,\frac{12\,\text{V} + 2\,(0.7\,\text{V})}{230\,\text{nH}} = 0.29\,\text{A}. \tag{31}$$

The maximum peak-to-peak current ripple would then be approximately 7.4 A, as increased from 7.1 A, if the deadtime is considered.

TABLE II
CIRCUIT COMPONENTS USED FOR LOSS ESTIMATION

Component	Part Number	Key Parameters
M1-M4	BSC011N03LSI	Rds=1.1mΩ Qg=20nC
M5-M7	BSC009NE2LS5I	Rds=0.95mΩ Qg=17nC
Inductor	SLR1075-231	L=230nH DCR=0.29mΩ
Cf1	10x10µF Ceramic	ESR=1.5mΩ
Cf2	10x47uF Ceramic	ESR=0.75mΩ
Input Capacitor	10x10µF Ceramic	ESR=1.5mΩ

V. LOSS ESTIMATE AND SIMULATION RESULTS

In order to properly design the ZIV converter, it is critical to understand the dominant sources of loss in the topology to achieve the maximum possible efficiency and power density. Despite being a hard-switching topology that does not rely on any resonant operation, the dominant source of loss in the ZIV converter is conduction loss. This is due to two key advantages of the topology. First, the figure of merit for a MOSFET is proportional to the maximum V_{ds} rating of the MOSFET. Therefore, the multilevel structure of the ZIV converter that reduces the MOSFET voltage stress allows for MOSFETs with lower ON-state resistance and gate charge to be used, reducing the switching and conduction losses. Second, the inductor voltage is only the flying capacitor ripple voltage. This allows for inductors as small as 230 nH to be used at 60 kHz switching frequency. Due to the very small size of the inductor, the magnetic losses are nearly negligible, with only the DCR inductor loss having any substantial impact on overall efficiency. The loss estimation presented in Fig. 12 was performed with the components given in Table II for an input voltage of 48 V, a load current of 25 A, and a switching frequency of 60 kHz. The conduction losses make up nearly 80% of the total converter loss at this load condition. It should be noted that the conduction loss will be proportionally higher at the full load condition of 35 A presented in Section VI.

The conduction loss of the MOSFETs can be estimated based on the load current of the converter and the ON-state resistance of the MOSFET as

$$P_{\text{cond}} = I_{\text{RMS}}^2\, R_{\text{DS(on)}}. \tag{32}$$

The four first-stage MOSFETs M1–M4 all operate with a duty cycle of 25% and carry the full load current for this time. In order to simplify the estimation, the load current can be assumed to be constant. This estimation is validated by the simulation and experimental results presented in Sections V and VI. The rms

TABLE III
COMPONENT VALUES AND CIRCUIT PARAMETERS USED FOR SIMULATION

Parameter	Value
Input Voltage	48V
Output Voltage	12V
Load Current	25A
Switching Frequency	60kHz
Capacitor 1	65µF
Capacitor 2	150µF
Inductor	230nH
Output Capacitor	150µF

TABLE IV
800 W/IN^3 EXPERIMENTAL PROTOTYPE COMPONENTS

Component	Value/Part Number
Input Capacitor	16x4.7µF 100V X7S 1210
First Flying Capacitor (C_{fl})	14x10µF 50V JB 1206
Second Flying Capacitor (C_{f2})	10x47µF 25V X5R 1210
Output Capacitor (C_{out})	10x47µF 25V X5R 1210
M1-M4	30V BSC011N03LSI
M5-M7	25V BSC009NE2LS5I
Inductor	230nH SLR 1075-231KE
Switching Frequency	60kHz

current for these MOSFETs is then given by

$$I_{\mathrm{RMS(M1-M4)}} = \sqrt{0.25}\ I_{\mathrm{load}} = 0.5 I_{\mathrm{load}}. \tag{33}$$

The three second-stage MOSFETs M5–M7 operate with a 50% duty cycle and carry the full load current for this time. The rms current for these MOSFETs is then given by

$$I_{\mathrm{RMS(M5-M7)}} = \sqrt{0.5}\ I_{\mathrm{load}} \approx 0.71 I_{\mathrm{load}}. \tag{34}$$

A simulation was used to verify the operation of the proposed circuit topology with the parameters listed in Table III. Note that the parameters in Table III approximate the "in-circuit" values of the components used in the experimental prototype as outlined in Table IV. The ceramic flying capacitors derate when holding a dc voltage, and the manufacturer derating curves were used to estimate the simulation parameters. Also note that in order to improve the readability of the waveforms, deadtime is neglected in the simulation. As shown by the loss analysis, inductor analysis, and the experimental waveforms, the overall impact of deadtime on the converter operation is low, as the deadtime is kept very short by design (on the order of nanoseconds) and the switching frequency of the converter is also low (below 100 kHz).

Fig. 13 shows the converter output voltage and the voltage of the two flying capacitors. From this figure, it can be seen that the first flying capacitor maintains its voltage at 0.5 V_{in} or 24 V, the second flying capacitor maintains its voltage at 0.25 V_{in} or 12 V, and the output voltage is equal to 0.25 V_{in} or 12 V. Fig. 14 shows the inductor voltage and the capacitor ripple voltage waveforms. Note that the capacitor ripple voltages are obtained by subtracting the nominal dc values of 0.5 V_{in} and 0.25 V_{in}, respectively. The inductor voltage is shown to be equal to the sum of the capacitor ripple waveforms. Note that as the capacitors alternate between charging and discharging depending on the current switching state, the inductor voltage is not a simple summation of these two waveforms, but rather the polarity of the capacitor voltage must be considered as shown in (1)–(3).

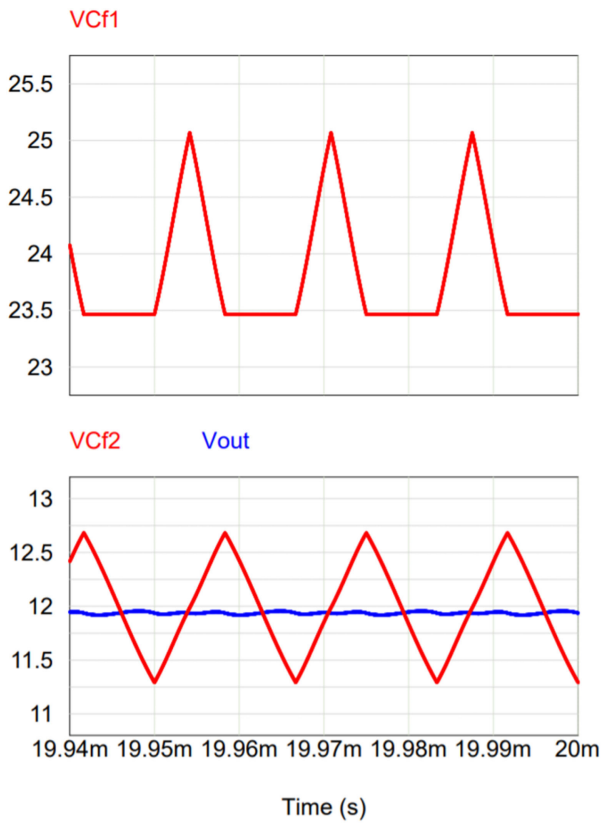

Fig. 13. Flying capacitor voltage and output voltage waveforms.

Fig. 15 shows the two flying capacitor current waveforms as well as the inductor current waveform. Note that for 25 A load, the expected rms current of the first-stage MOSFETs, assuming no inductor ripple, is 12.5 A from (33), and the expected rms current for the second stage MOSFETs is 17.7 A from (34). From the simulation, including the inductor ripple, the first-stage MOSFET rms current is 12.53 A, and the second-stage MOSFET rms current is 17.74 A.

VI. EXPERIMENTAL RESULTS

A prototype was constructed using the components outlined in Table II. The experimental results presented in this section were gathered with an input voltage of 48 V, a switching frequency of 60 kHz, and a nominal load current of 25 A. For the experimental setup, the input power is supplied by a Chroma dc supply, and the load is a Chroma dc load. The gate drive and MCU power are supplied by an auxiliary power supply providing 8 V gate drive voltage. The waveforms are measured with a Tektronix oscilloscope. The converter is operated with a switching frequency of 60 kHz. For the first prototype, the efficiency measurements are calculated using a Keithley 2700 digital multimeter to measure the input and output voltages and the input and output current readings from the supply and load. In order to improve the measurement accuracy for the second prototype efficiency measurements, all currents are measured using a Reidon RSN

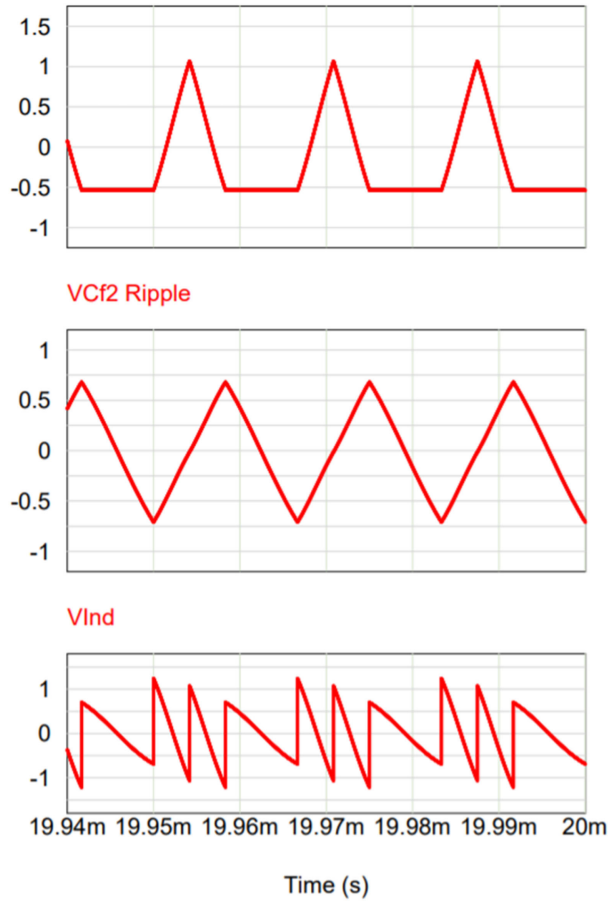

Fig. 14. C_{f1} voltage ripple (top), C_{f2} voltage ripple (middle), and inductor voltage (bottom) waveforms.

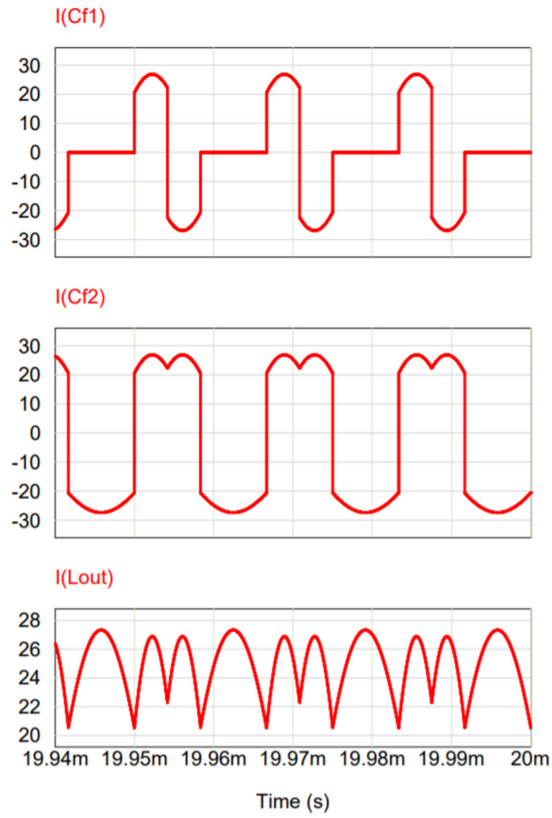

Fig. 15. Flying capacitor and inductor current waveforms.

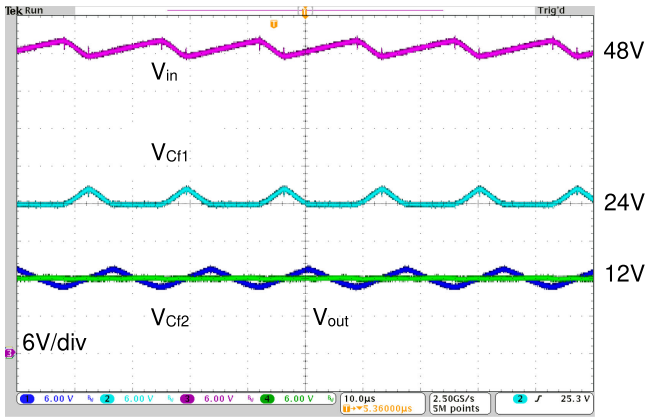

Fig. 16. Converter input voltage, C_{f1} voltage, C_{f2} voltage (dark blue), output voltage (green) at 12 V/25 A load.

series (0.1% error) current shunt and a Keithley 2700 digital multimeter. This Keithley digital multimeter is also used to take all of the voltage measurements. For cooling the second, smaller prototype above 20 A output current, a 4 in USB powered desk fan is used.

Fig. 16 shows the converter input voltage, the voltage of the two flying capacitors, and the output voltage. For the 48 V input voltage, the flying capacitor is charged to 0.5 V_{in} or 24 V, the second flying capacitor is charged to 0.25 V_{in} or 12 V, and the output voltage is also 0.25 V_{in} or 12 V. This figure shows excellent agreement with the simulation waveforms presented in Fig. 13.

Fig. 17 shows the inductor current (top) and inductor voltage (bottom) waveforms. The shapes of the inductor current and voltage waveforms closely match the results expected from the simulation. As discussed in Section IV-B, the practical ZIV converter requires deadtime between switching transitions to prevent shoot-through. This can be seen in Fig. 17, as the inductor sees a negative voltage during this deadtime. However, the deadtime in the circuit is extremely short, on the order of 10 s of nanoseconds. Therefore, as seen in the current waveform, the impact of this deadtime on the overall inductor current ripple is almost negligible. This inductor waveform also shows the MOSFET currents, as the inductor current will be equal to the current through the ON-state MOSFETs. This current measurement, therefore, validates the rms current estimates based on the circuit analysis and simulation results.

Fig. 18 shows the ripple voltage for both flying capacitors at 25 A load current.

Fig. 19 shows the voltage stress waveforms for MOSFETs M1 and M5. From this figure, it can be seen that the voltage stress of the first MOSFET, M1, is reduced to approximately 0.5 V_{in} or 24 V, with the peak stress value varying a small amount due to the capacitor voltage ripple as per (25). It can also be seen that the voltage stress of the M5 MOSFET is reduced to approximately

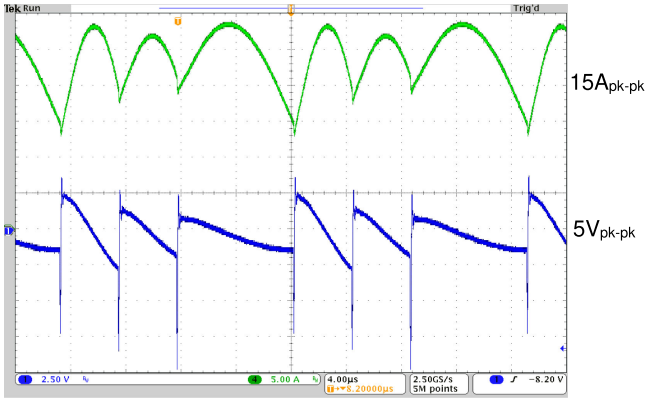

Fig. 17. Inductor current (top) and inductor voltage (bottom) waveforms at 12 V/25 A output load.

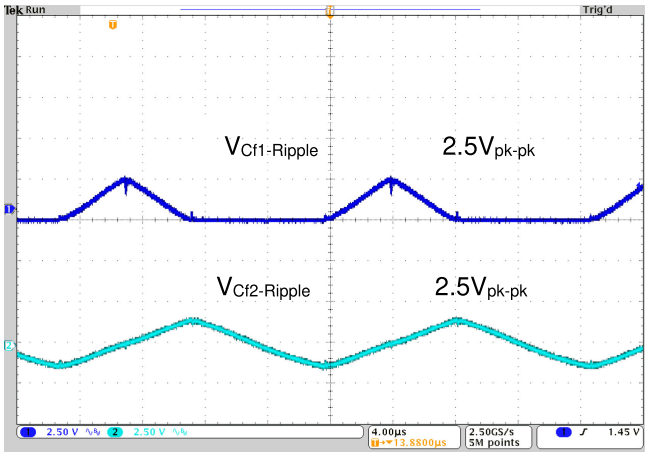

Fig. 18. Flying capacitor ripple voltage waveforms at 12 V/25 A output load.

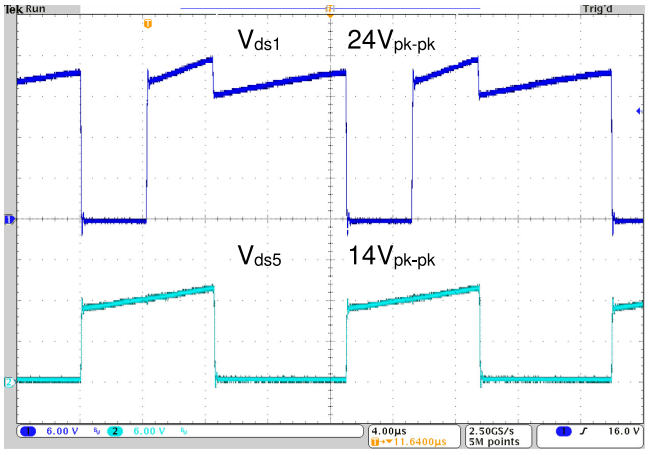

Fig. 19. MOSFET M1 (top) and M5 (bottom) drain-to-source voltage waveforms.

14 V, with the peak stress value increased slightly from the expected value of 0.25 V_{in} (12 V) by the capacitor ripple. There is also very little ringing present in the V_{ds} waveforms for M1 and M5. It is important when designing the circuit layout that the parasitic inductance in the power circuit be kept sufficiently

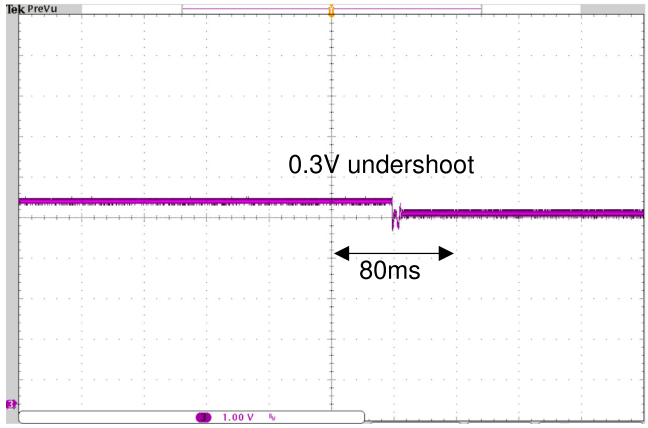

Fig. 20. Output voltage waveforms of 5 V for load step of 1 to 20 A.

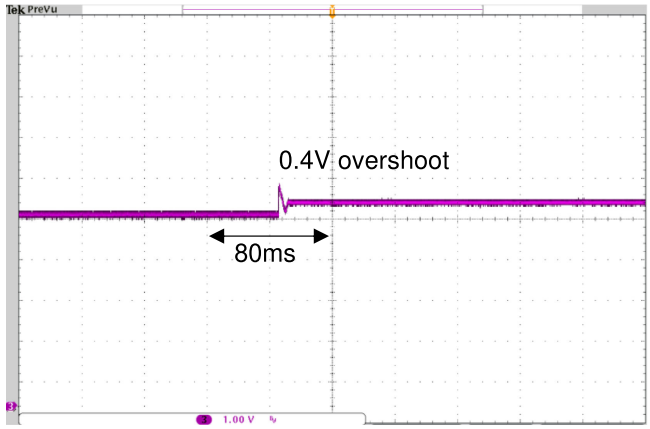

Fig. 21. Output voltage waveforms of 5 V for load step of 20 to 1 A.

small so that the capacitor ESR and MOSFET ON-resistance can damp it effectively. If the layout is not designed correctly and the parasitic inductance is too large, the voltage stress on the MOSFETs may increase due to ringing, requiring higher voltage rated devices, or potentially damaging the circuit.

The load transient response is shown in Figs. 20 and 21. In this test, the input voltage is 20 V, for an output voltage of 5 V. The load is stepped from 1 to 20 A with a slew rate of 10 A/μs (the maximum possible with the testing equipment available). There is very little overshoot and undershoot present in the output voltage waveform. The reduction in output voltage is due partly to the resistive drop throughout the circuit, but it should be noted that the power supply is connected to the board through a long wire, and the voltage drop across this wire is not negligible. Thus, part of the output voltage sag is due to the reduction in the input voltage seen at the board's input terminals.

The measured efficiency of this experimental prototype, including the gate drive loss, is shown in Fig. 22 in red. The peak efficiency is above 99.5% and the full load efficiency at 12 V/35 A (420 W) output is 98.1%. The efficiency without considering gate drive loss is also presented in blue.

The start-up waveform for the converter prototype is shown in Fig. 23, with the input voltages C_{f1} and C_{f2}. For this experiment, the input voltage is increased from 0 V to the nominal 48 V

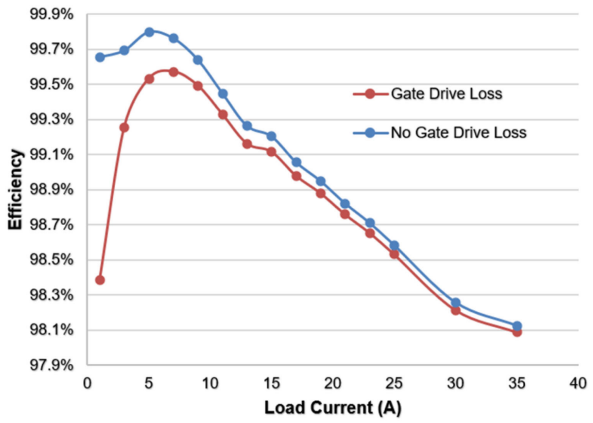

Fig. 22. Measured prototype efficiency including gate drive loss (red) and neglecting gate drive loss (blue).

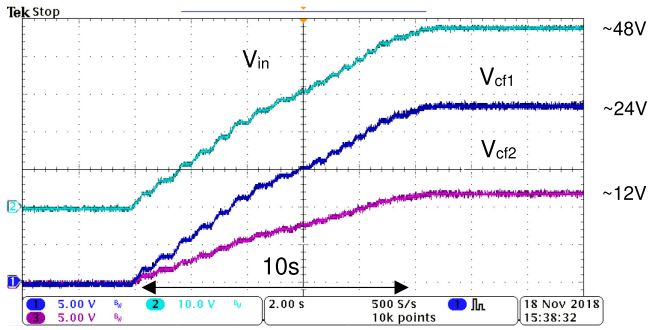

Fig. 23. Converter input voltage and flying capacitor voltage waveforms during start-up.

value manually over a period of approximately 10 s. It should be noted that no active capacitor balancing or control circuitry is added to the circuit; therefore, this procedure also validates the claim that the capacitors will naturally balance near their expected value based on the duty cycle of the MOSFETs, as the capacitors naturally correct for the "imbalance" created when the input voltage is stepped and settle to their nominal values of 0.5 and 0.25 V_{in}, respectively.

This initial prototype was designed as a proof of concept and, thus, was relatively large, with additional space allocated for testing and measurements. A second much smaller prototype was designed later, as shown in Figs. 24 and 25. This prototype achieves a power density of 800 W/in^3. The components selected for this prototype are shown in Table IV. The dimensions of the prototype are 0.9" width, 1.3" length, and 0.45" height as measured by the tallest component on both sides of the board, namely the inductor on the top side of the board. It should be noted that the flying capacitors used in this design are larger than the minimum values estimated in 26 and 27. These larger values were selected for two reasons. First, as previously mentioned, the flying capacitor ESR is a significant source of loss at high-current levels. Therefore, utilizing the minimum capacitor values would reduce the converter efficiency. Additionally, the physical layout of the circuit is designed to minimize the parasitic loop inductances in the current paths of the circuit. When the MOSFETs are arranged in this configuration, the width and length of the

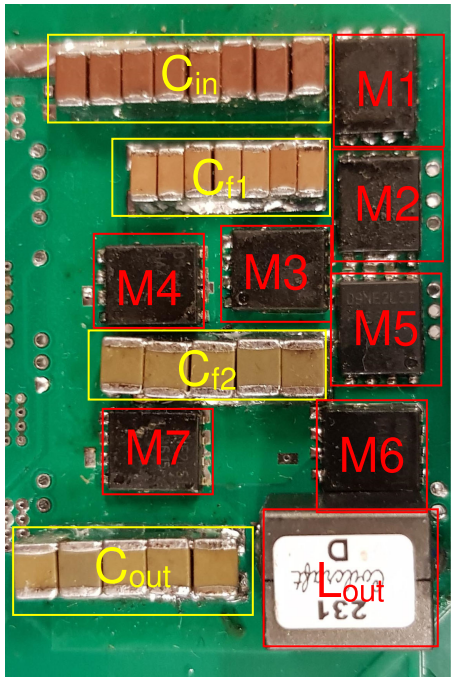

Fig. 24. 800 W/in^3 (width 0.9", length 1.3", height 0.45") experimental prototype top view with power components labeled.

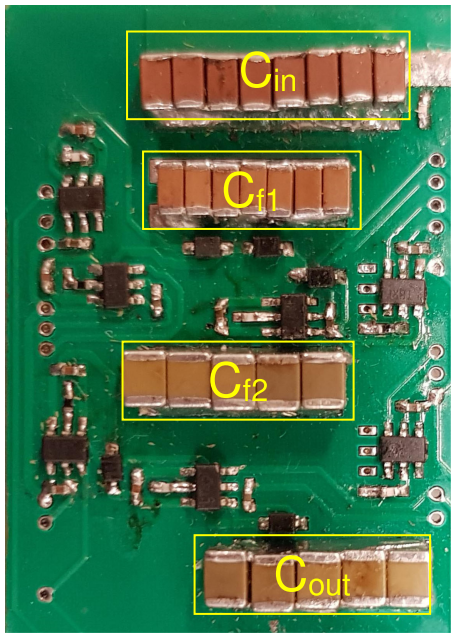

Fig. 25. 800 W/in^3 (width 0.9", length 1.3", height 0.45") experimental prototype bottom view with power components labeled.

board are primarily dominated by the layout of the MOSFET packages. The flying capacitor banks are then added in to fill the leftover space on the board, as can be seen in Figs. 24 and 25. In this particular design, removing some of the flying capacitors would not allow for any reduction in size and would reduce the efficiency of the prototype.

The accuracy of the efficiency measurements for this prototype was also improved, using Reidon RSN series (0.1% error)

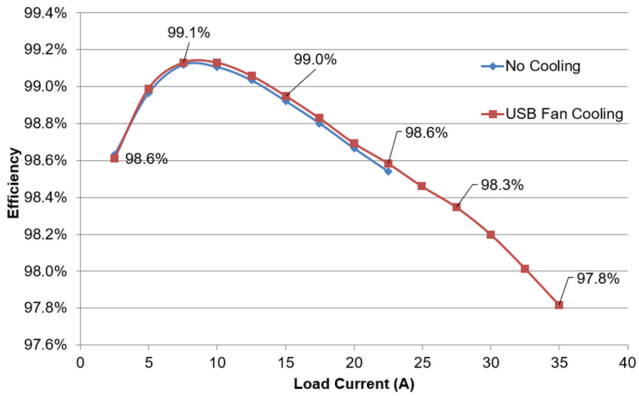

Fig. 26. 800 W/in^3 experimental prototype measured efficiency including gate drive loss.

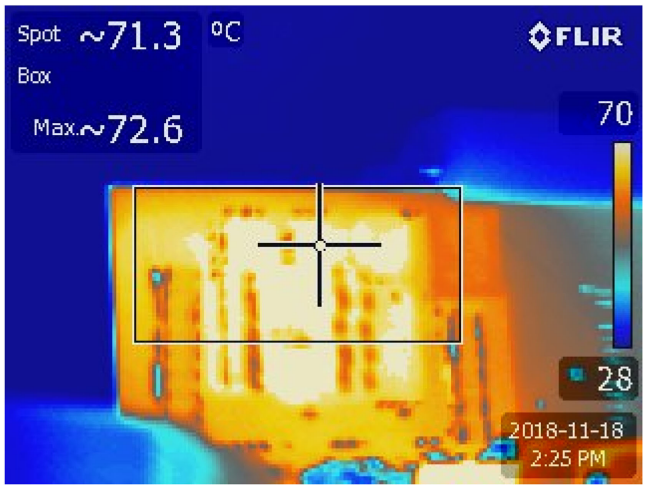

Fig. 27. 800 W/in^3 experimental prototype thermal image 12 V/17.5 A half-load condition with no fan cooling.

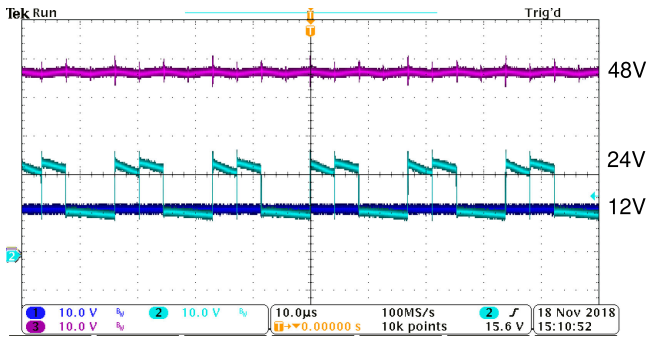

Fig. 28. Input voltage, Node 1, and output voltage waveforms for 12 V/15 A load.

current shunts as well as a Keithley 2700 digital multimeter for higher measurement accuracy. Due to this second prototype's smaller size, a 4 in USB desk fan was used for cooling to achieve the maximum rated output current of 35 A.

The efficiency measurements for the second prototype are presented in Fig. 26. The curve in blue shows the efficiency measurements with no fan cooling, and the curve in red shows the

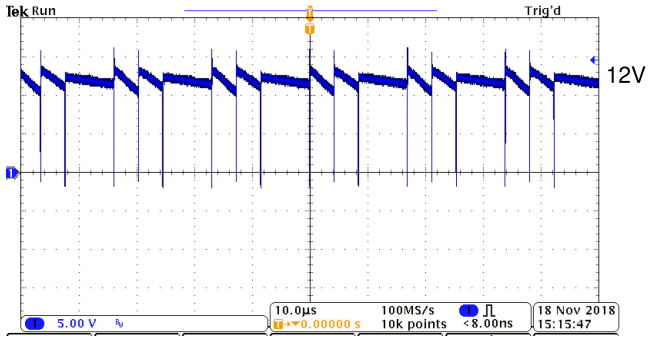

Fig. 29. Node 2 voltage waveform for 12 V/15 A load.

efficiency measurements with the fan cooling. For both curves, gate drive loss is included in the efficiency measurements. The peak efficiency for this prototype is measured to be 99.1%, with a full load of 12 V/35 A efficiency of 97.8%.

Fig. 27 shows a thermal image of the prototype operating at 12 V/17.5 A half-load condition with no fan cooling. Fig. 28 shows the input voltage, Node 1 voltage, and output voltages for the converter operating at 12 V/15 A load. Fig. 29 shows the Node 2 voltage waveform.

VII. Conclusion

In this article, a novel intermediate bus converter topology has been proposed. The topology achieves an extremely high peak efficiency of over 99%, as well as a full load 97.8% efficiency for 420 W output with a power density of 800 W/in^3. The key drivers of the very high performance achieved by this topology are the multilevel structure, which allows for lower MOSFET voltage stress, and therefore much lower figure-of-merit MOSFETs to be used, and the unique feature that the inductor voltage of the converter does not depend on the input or output voltage values. Through the ZIV operation, the proposed topology can utilize inductors as small as 230 nH, while also operating at low switching frequencies, such as 60 kHz. This means that, despite being a hard-switched topology, the frequency-related losses are minimized and conduction loss is the dominant source of loss in the topology. Magnetic losses are also almost entirely eliminated. Unlike many SCC topologies, all the capacitors in the ZIV converter are naturally soft-charged and the converter is not sensitive to any particular component tolerances, as there is no sensitive resonant operation. This makes the ZIV converter highly scalable and straightforward to design for demanding high-current applications.

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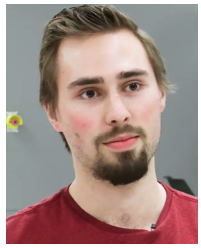

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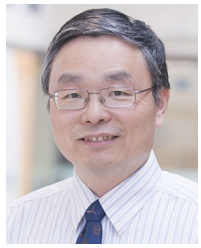

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