Accurate Analysis and Design of the Circuit Parameters of *LLC* DC–DC Converter With Synchronous Rectification

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***Abstract*—In high-load-current *LLC* dc–dc converter, synchronous rectification (SR) is usually used to reduce the secondary loss. As a lossless, low-cost, and small-volume SR control strategy, the drain–source voltage of SR switches sensing method is used widely in industrial applications. However, when the load current increases, the voltage ringing across SR switches during O stage is more and more severe and reaches zero eventually. When the voltage ringing reaches around zero in *LLC* converter, the voltage-sensing-method SR controller will generate the false driving signal, which makes SR switches turn ON early and causes the converter works abnormally. This article presents the accurate analysis and design of the circuit parameters of *LLC* dc–dc converter to prevent the voltage ringing across the SR switches reaches around zero. The voltage ringing model is established, and the parameters design principle is given. By using the proposed design guideline, the voltage ringing across SR switches will always be higher than zero over the full load range, which eliminates the turn-ON early issue or turn-ON several times in one cycle issue. Therefore, this article can provide a design reference and guideline for the high-load-current and high-output-power *LLC* converter with voltage sensing SR control strategy. A 2.16 kW SR *LLC* dc–dc converter prototype is built according to the proposed design guideline, and the experimental results verify the correctness and effectiveness of the analysis.**

***Index Terms*—*LLC* dc–dc converter, parameters design, synchronous rectifier, turn-ON early.**

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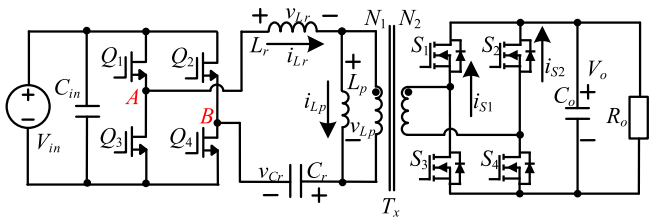

Fig. 1. Full-bridge *LLC* converter with SR.

I. Introduction

LLC resonant converter is becoming more and more popular as both zero-voltage switching (ZVS) of the primary-side switches and zero-current switching of the secondary-side rectifiers can be achieved [1]. Along with the maturity and widespread application of the wide bandgap devices, the higher switching frequency, power density, and efficiency become the developing trend of the *LLC* converters. As the switching frequency is high, the parasitic parameters have an increasing effect on the performance of the *LLC* converter. The voltage oscillation of the *LLC* resonant converter caused by the parasitic parameters under light load is studied in [2]–[4]. Wu and Shi [5] reveal that the parasitic parameters of the switches in the *LLC* converter are the key parameter for determining the primary conduction losses. In [6]–[10], the various optimal parameters' designs of *LLC* converter are presented to improve the performance of the efficiency, switching frequency range, and voltage gain.

In decades, *LLC* resonant converters are used widely in many different applications. The typical applications for *LLC* converters are electric vehicles' applications, renewable generation systems, data center applications, etc. In these applications, the converters usually operate with a low output voltage and a high load current [11], [12]. As the conduction loss is related to the square of rms current, the transformer secondary conduction loss is dominant as the secondary current stress is high. Because the ON-state resistance of the switch ($R_{ds,\mathrm{on}}$) is very small, and the product of the $R_{ds,\mathrm{on}}$ and the current flowing through the switch is much smaller than the forward voltage V_F of the diode. Therefore, synchronous rectification (SR) can reduce the conduction loss significantly [12], [13].

The full-bridge *LLC* converter with SR is shown in Fig. 1. To improve further efficiency of the *LLC* converter, an optimal SR

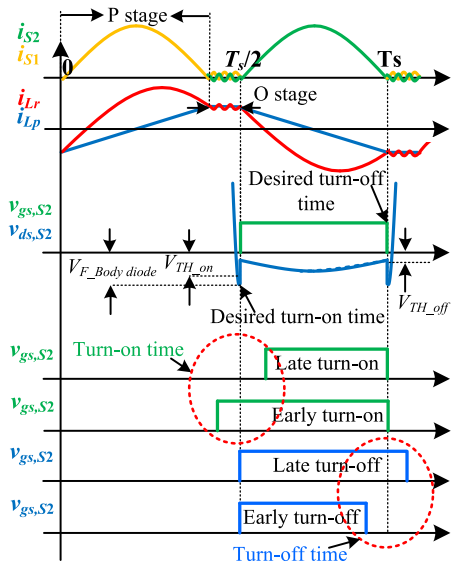

Fig. 2. Issues when the SR switches are turned ON and turned OFF.

control is required to keep the SR switches always conducting when the secondary current flows to load and avoid a long conduction time of the body diode [13]. However, there are some issues when the SR switches are turned ON and turned OFF.

From Figs. 1 and 2, during the time 0 to $T_s/2$, when the voltage across inductor L_p is positive clamped and the voltage $v_{Lp} = nV_O$, this operation stage is denoted as P stage. When the voltage across inductor L_p is negative clamped and the voltage $v_{Lp} = -nV_O$, this operation stage is denoted as N stage. When the voltage across inductor L_p is not clamped and the secondary switches are turned OFF, this operation stage is denoted as O stage. Generally, the *LLC* converter could operate in six major modes, which are PO, PON, PN, NP, NOP, and OPO [6], and PO mode is shown in Fig. 2. As the voltage ringing generally occurred during O stage, only the operation mode including O stage is analyzed in this article. NOP mode suffers the reverse recovery current problem; thus, this stage is not designed in the proposed prototype to optimize the efficiency. In PON mode, the O stage is short; thus, the voltage ringing has a limit effect on the converter even if the SR switches are turned ON early. OPO mode exits in light-load condition, and the voltage ringing is not severe according to the theoretical analysis in this article. Therefore, the PO mode is selected as an example to analyze in this article.

Fig. 2 shows the late turn-ON, early turn-ON, late turn-ON, and early turn-OFF four issues in the *LLC* converter with SR. For these issues, current sensing, voltage sensing, and theoretical calculation are the three main methods that are proposed to make the SR switches conduct properly and achieve optimal efficiency.

A. Late Turn-ON Issue

In *LLC* converter, the transformer secondary current flows through the rectifier to the load during P stage, and there is no current flowing through the rectifier during O stage [14]. At the beginning of the P stage, the parasitic output capacitance of the SR switches needs to be discharged to achieve ZVS turn-ON. As the transformer secondary current is small at the beginning of the P stage under light load, a long time is required to discharge the output capacitance of the SR switches fully. In [15], the SR switches turn-ON signal is synchronized with the primary-side gate signal with a small delay by considering the microchip delay. If the delay time is too short, ZVS turn-ON of the SR switches cannot be achieved. If the delay time is too long, the SR switches will be turned ON late and cause a large loss due to the long conduction time of the body diodes of the switches.

In [16], the secondary current is sensed to generate a proper driving signal of the SR switches by the current transformers (CTs). However, the transformer secondary current stress is high. Thus, the CTs will cause extra loss and cost, which is unsuitable for secondary current sensing. The low-current-stress primary current is detected in [17] and [18] to reduce the conduction loss of CTs. As the primary resonant current cannot reflect the rectifier current due to the magnetizing current, an extra compensating winding is required to cancel out the magnetizing current [17], [18]. The auxiliary winding and the detecting circuits are proposed in [19] and [20] to emulate the secondary rectification current by using the lossless and impassive components. But it still increases the complexity and cost of the converter.

Although the current sensing can make SR switches conduct well, it is not a popular method due to extra loss, cost, and bulky. The voltage sensing is used in many industrial applications as only the voltage across the drain to the source of the SR switches is required to detect, which benefits from no extra loss, small volume, and cheap. As shown in Fig. 2, at the end of the O stage, the voltage $v_{ds,S2}$ decreases. When the voltage $v_{ds,S2}$ decreases to the voltage of body diodes $-V_F$ at the beginning of the P stage, the voltage $v_{ds,S2}$ is lower than the threshold voltage $V_{\mathrm{TH,on}}$, then the SR switches are turned ON. Along with the transformer secondary current decreasing to zero, the voltages across SR switches are higher than the threshold voltage $V_{\mathrm{TH,off}}$, then the SR switches are turned OFF.

In industrial applications, many manufacturers propose the voltage sensing chips for the SR due to high efficiency, low cost, and stable performance, for example, SRK2000A of the ST, NCP4305 of the Onsemi, UCC24624 of the TI, TEA1795T of the NXP, and MP6924 of the MPS.

B. Early Turn-OFF Issue

For the *LLC* converter with a short fixed conduction time of SR switches over full load range and input voltage conditions, the early turn-OFF issue is occurring as the P stage time changes along with load and input voltage changes [21].

As mentioned above, voltage sensing is an economical and reliable method to solve abnormal turn ON or OFF. However, due to the stray inductance in both the PCB traces and the SR switches package, the voltage across the stray inductance is also detected, which causes the SR switches turn-OFF early and increases the loss of body diodes of SR switches [13]. To solve this problem and improve the efficiency of the converter, Wang et al. [22]–[24] proposed the auxiliary circuit to compensate

for the stray inductance, and SRs can be turned OFF properly with almost no body diode conduction. However, $R_{ds,\mathrm{on}}$ is not constant at different current stresses, temperatures, driving voltages, etc. Thus, the compensation circuits are not precise at all the operating conditions.

In [25] and [26], the digital detecting methods for the SR switches are proposed based on the voltage sensing method. When the voltage of body diodes $-V_F$ is detected after the SR switches are turned OFF, it means that the SR switches are turned OFF early and the body diodes are turned ON. In the next cycle, the digital controller generates a longer conduction time for SR switches. When the voltage of body diodes $-V_F$ is not detected after the SR switches are turned OFF, it means that the SR switches are turned OFF properly. In the next cycle, the digital controller generates a shorter conduction time for SR switches. By using this control strategy, the conventional turn-OFF threshold voltage $V_{\mathrm{TH,off}}$ is not required to be detected. Thus, the early turn-OFF issues are solved in the conventional voltage sensing method, and the SR switches can be turned ON with almost no body diode conduction. To improve the steady-state performance and reliability during transients, the primary current is also sensed in [27] to generate an analytic–adaptive method based on the digital detecting of SR switches voltage.

A high-voltage sensing method is proposed in [28]. The resonant capacitor voltage is detected to control the SR switches. As the resonant capacitor voltage is high, the sensing circuit is complex and limited to the high voltage stress.

To remove the current or voltage sensing circuits and reduce the cost, Zhu et al. [15] and Ren et al. [29]–[33] build some accurate mathematical modes to calculate the turn-ON time, the turn-OFF time, and the conduction time related to the switching frequency and load condition, which makes the driving signals of SR switches adjusted adaptively. However, the precise information of the output voltage, the load current, and the input voltage is required to judge which operation stage of the *LLC* converter is. Thus, these methods are not suitable in the high-load-current applications as the precise load-current sensing still requires a lossy resistor sensor, complex detecting circuits, or bulky CTs.

C. Late Turn-OFF Issue

As shown in Fig. 2, if the SR switches still conduct after the end of P stage, the load current would flow from the drain to the source of the SR switches; thus, the output energy would be transferred back to the primary side. In [34] and [35], when the secondary switches are turned OFF late than the primary switches, the circulating energy caused by a reverse current increases rms currents, which deteriorate the efficiency of the converter. In addition, a large reverse current increases the turn-OFF current and induce a huge drain spike, which increases the switching loss and voltage stress of the secondary switches [36].

For *LLC* converter, under the very light-load condition, there is an unintended increase of output voltage beyond the regulation limit, and the output voltage is difficult to regulate even if the converter operates at a very high switching frequency [37]. In [38], the regulation capability can be improved and the output voltage is stable under a very light load by using the reverse current. By adjusting the turn-OFF delay time to control the reverse current, the output energy can be transferred to the primary side; thus, the voltage gain can be reduced. Therefore, a lower switching frequency can regulate the output voltage under the light load, which reduces the switching loss and driver loss significantly.

D. Early Turn-ON Issue

Similar to the late turn-OFF issue, the early turn-ON issue also causes the reverse current and increases rms currents and conduction loss. However, the relevant past works of early turn-ON issues are scarce.

As mentioned above, lots of voltage sensing Integrate Circuit (ICs) are proposed by the main power management companies due to lossless, low cost, and stable performance. Thus, voltage sensing ICs are very popular for SR switches in industrial applications. However, a severe voltage ringing occurs during O stage due to the resonant components and the parasitic parameters. If the voltage sensing ICs are used to generate the driving signal for SR switches, a voltage ringing will lead to the early turn-ON issue [39].

As a severe voltage ringing causes the voltage across the SR switches reaches to zero several times during O stage, in [10] and [34], the calculated control strategy is used for the primary and secondary switches by the digital controller; thus, the SR switches can be turned ON correctly. A turn-ON delay time longer than the O stage time is designed in [36] to prevent the permuted turn-ON of SR switches and the leading edge inversion current. However, when there is no voltage ringing across SR switches, a long turn-ON delay time will make the body diodes of SR switches conduct and increase the conduction loss. The control of a variable turn-ON delay time is proposed in [36], but it still increases the cost and complexity of the controller as the leading edge inversion current is required to be detected. In [40], the polarity of the voltage across the transformer is detected to judge that SR switches should be conducted in P stage instead of O stage, which eliminates the misconducting of the SR switches caused by the voltage sensing ICs detecting voltage ringing. Similarly, the polarity of the resonant current is obtained by detecting the inductor voltage to avoid the false driving pulses problem caused by the oscillation in O stage [41]. However, in these methods, the polarity is hard to determine due to the oscillation of the rectifier voltage. In addition, extra sensing circuits are required, which increases the cost and the complexity compared to only using the voltage sensing ICs.

In some voltage sensing ICs, the minimum turn-ON and turn-OFF time can be set to avoid the oscillation closed to the threshold turn-ON or turn-OFF voltage [42]. However, it is still difficult to design a proper fixed minimum turn-ON and turn-OFF time that can be used over the full load and input voltage ranges.

Fig. 3(a) shows that the voltage sensing method IC is used in the SR *LLC* converter in Fig. 1. In Fig. 3(b), if the minimum turn-ON time is longer than the O stage time, the switches S_1 and

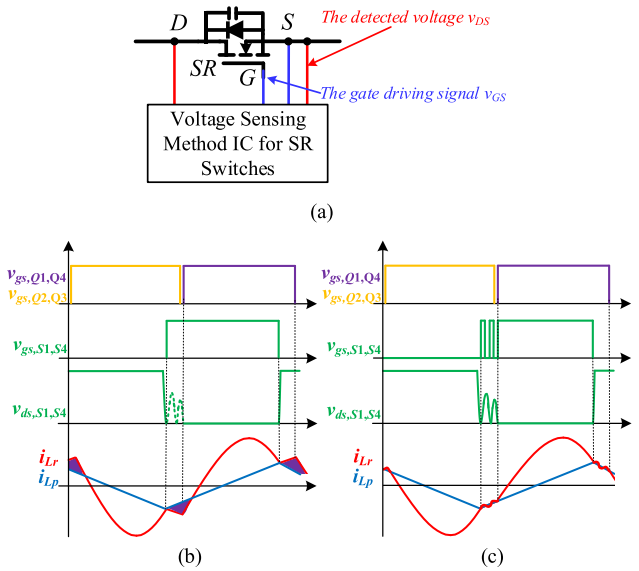

Fig. 3. Waveforms of the SR *LLC* converter when (a) voltage sensing method IC is used, (b) minimum turn-ON time is too long, and (c) minimum turn-ON time is too short.

S_4 are turned ON when $v_{ds,S1}$ and $v_{ds,S4}$ decreases to $-V_F$ for the first time at O stage, which causes the early turn-ON issue and reverse current shown with purple block. As shown in Fig. 3(c), if the minimum turn-ON time is shorter than the oscillation time, the switches S_1 and S_4 are turned ON when $v_{ds,S1}$ and $v_{ds,S4}$ decrease to $-V_F$ every time at O stage, which causes the SR switches to switch several times during one cycle and increases the switching loss significantly. As the switching frequency range of the *LLC* converter is wide, the O stage time range is very wide. Thus, a proper minimum turn-ON time is difficult to design. Corresponding to the theoretical waveforms in Fig. 3, the SIMPLIS simulated waveforms of the *LLC* converter with the voltage sensing method IC NCP4305 are shown in Fig. 4. The waveforms in Fig. 4 are consistent with that in Fig. 3, which verifies the early turn-ON issue by using the voltage sensing ICs in the *LLC* converter.

In summary, if we want to use only the voltage sensing ICs and eliminate the issues, as shown in Figs. 3 and 4, an effective and useful method is the voltage ringing during O stage that should be studied and a severe voltage ringing is eliminated by an optimal design of the circuit parameters.

In this article, the accurate analysis and design of the circuit parameters of *LLC* dc–dc converter with SR is proposed to avoid the voltage ringing reaching zero during O stage. Thus, the early turn-ON issue can be solved, and the voltage sensing ICs can be used directly to drive the SR switches well, which simplifies the driving circuit and control strategy of the SR switches. The rest of this article is organized as follows. The analysis of the voltage across SRs is presented in Section II. Section III proposes the optimal design of the circuit parameters to avoid the turn-ON early issue of the SR switches. The simulated and experimental verification is shown in Sections IV and V. Finally, Section VI concludes this article.

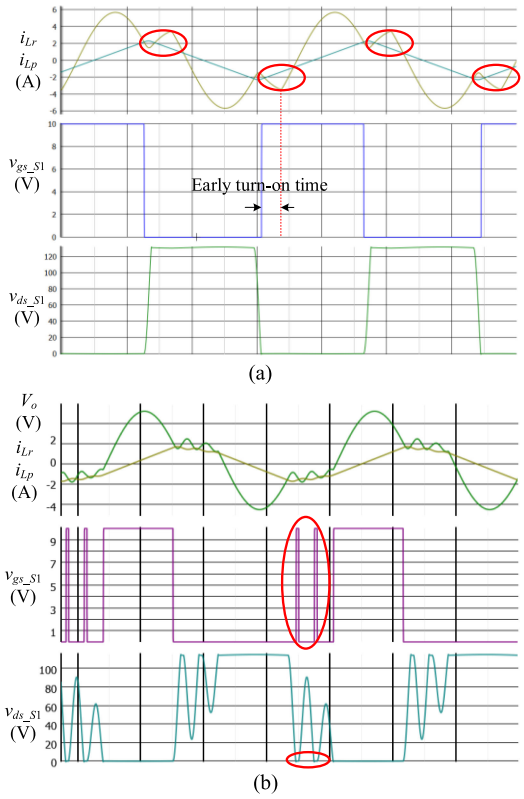

Fig. 4. SIMPLIS simulated waveforms of the *LLC* converter with the voltage sensing ICs NCP4305. (a) Minimum turn-ON time is too long. (b) Minimum turn-ON time is too short.

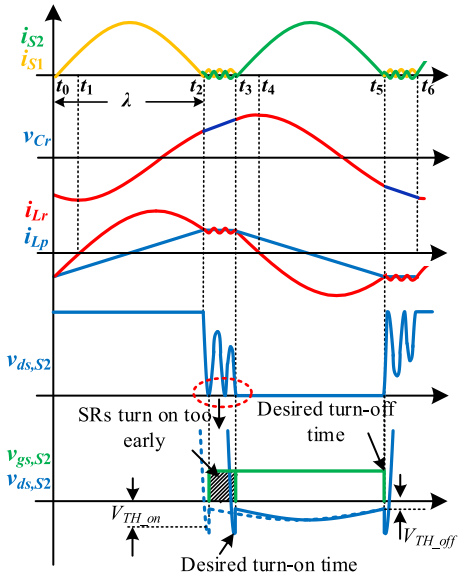

Fig. 5. Key waveforms of the *LLC* converter with SR.

II. Analysis of the Voltage Across SR Switches

Fig. 5 shows the key waveforms of the *LLC* converter with SR by using the voltages sensing ICs.

As shown in Fig. 5, during O stage (t_2–t_3), there is voltage ringing across the SR switches, such as $v_{ds,S2}$. In *LLC* converter,

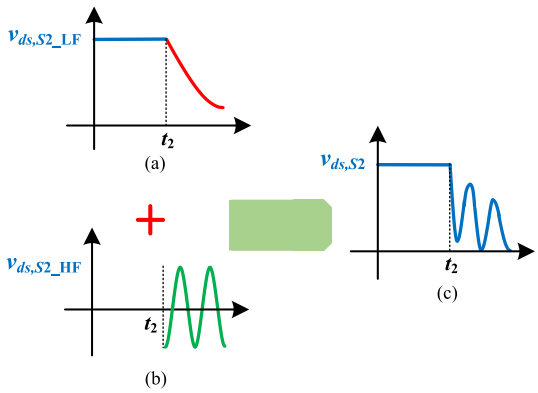

Fig. 6. Synthesis of the voltage ringing across the SR switches. (a) Low-frequency component. (b) High-frequency component. (c) Synthesized voltage ringing across the SRs.

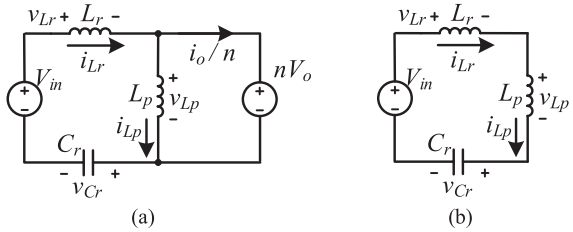

Fig. 7. Equivalent circuit of the *LLC* dc–dc converter at (a) P stage and (b) O stage.

the SR switches are always turned-OFF during O stage, and there is no energy that is transferred from the transformer primary to the secondary. However, for the *LLC* converter with voltage sensing SR controller, if the voltage ringing across the SR switches reaches threshold voltage $-V_{\mathrm{th,on}}$ for several ten nanoseconds continuously, the gate driving signals of the SR switches are generated by the SR controller. Then, the SR switches are turned ON early, and the energy is transferred back to the transformer primary from the transformer secondary, which makes the circuit work abnormally. In Fig. 5, the $v_{ds,S2}$ shown with dashed line presents the real waveforms caused by the voltage ringing, and the $v_{ds,S2}$ shown with solid line presents the desired turn-ON gate driving signal, and the shaded area presents the turn-ON early time.

To solve the turn-ON early issue of the SR switches, the voltage ringing across SR switches is analyzed first. As shown in Fig. 6, since t_2, the voltage ringing across the SR switches is synthesized by the low-frequency component and the high-frequency component. The two components are analyzed in detail below.

A. Low-Frequency Component Analysis of the Voltage Ringing Across the SR Switches

During t_0–t_2 in Fig. 5, the equivalent circuit of P stage of the *LLC* dc–dc converter in Fig. 1 is shown in Fig. 7(a). During t_2–t_3 in Fig. 5, the equivalent circuit of O stage of the *LLC* dc–dc converter in Fig. 1 is shown in Fig. 7(b).

Defining that the K, the resonant angle frequency ω_r between L_r and C_r, and the resonant angle frequency ω_p between $(L_p{+}L_r)$ and C_r are

$$\begin{cases} K = \frac{L_p}{L_r} \\ \omega_r = \frac{1}{\sqrt{L_r C_r}} \\ \omega_p = \frac{1}{\sqrt{(L_r+L_p)C_r}}. \end{cases} \tag{1}$$

As shown in Fig. 5, $\lambda = t_2$-t_0 is the duration of P stage. To simplify the analysis, according to [43], λ can be approximated as

$$\lambda \approx \frac{f_s}{f_{r1}} \cdot \frac{T_s}{2} = \frac{\pi}{\omega_r}. \tag{2}$$

By using the analysis method in [6], the resonant capacitor voltage $v_{Cr,LF}(t)$ during t_2–t_3 can be obtained as

$$v_{C_r,LF}(t-t_2) = \left(-2nV_o + V_{\mathrm{in}} + \frac{V_o^2}{4C_r R_o V_{\mathrm{in}} f_s}\right) \times \cos\omega_p(t-t_2) + \frac{nV_o\pi\sqrt{K+1}}{2K}\sin\omega_p(t-t_2) + V_{\mathrm{in}} \tag{3}$$

where transformer turns ratio is $n = N_1{:}N_2$.

During t_2–t_3, the current i_{Lr} can be regarded as equal to i_{Lp}. Therefore, the magnetizing inductor voltage $v_{Lp,LF}$ can be calculated as

$$v_{L_p,LF}(t-t_2) = \frac{L_p}{L_p+L_r}[V_{\mathrm{in}} - v_{Cr,LF}(t-t_2)]. \tag{4}$$

According to Kirchhoff voltage laws (KVL), the low-frequency component of the voltage ringing across the SR switch S_2 $v_{ds,S2,LF}(t)$ during t_2–t_3 is

$$v_{ds,S2,LF}(t-t_2) = \left(V_o + \frac{v_{L_p}(t-t_2)}{n}\right)/2. \tag{5}$$

Substituting (3) and (4) into (5), the low-frequency component of the voltage ringing across the SR switch S_2 $v_{ds,S2,LF}(t)$ can be rewritten as

$$v_{ds,S2,LF}(t-t_2) = \frac{V_o}{2} - \frac{K}{2n(K+1)} \times \left[\begin{array}{l}\left(-2nV_o + V_{\mathrm{in}} + \frac{V_o^2}{4C_r R_o V_{\mathrm{in}} f_s}\right)\cos\omega_p(t-t_2) \\ + \frac{nV_o\pi\sqrt{K+1}}{2K}\sin\omega_p(t-t_2)\end{array}\right]. \tag{6}$$

B. High-Frequency Component Analysis of the Voltage Ringing Across the SR Switches

During t_2–t_3 in Fig. 5, the converter circuit is shown in Fig. 8(a) when the parasitic capacitance C_p of the transformer and the parasitic output capacitance C_{oss} of the SR switches are considered.

As the capacitance C_r is much higher than $(C_{oss}{+}C_p)/n^2$, the dc source V_{in} and V_o, and the capacitance C_r can be ignored when the high-frequency component of the voltage ringing across the SR switches is analyzed. Thus, the equivalent circuit of the converter during t_2–t_3 is shown in Fig. 8(b). Defining that the C_e is

$$C_e = (C_{oss} + C_p). \tag{7}$$

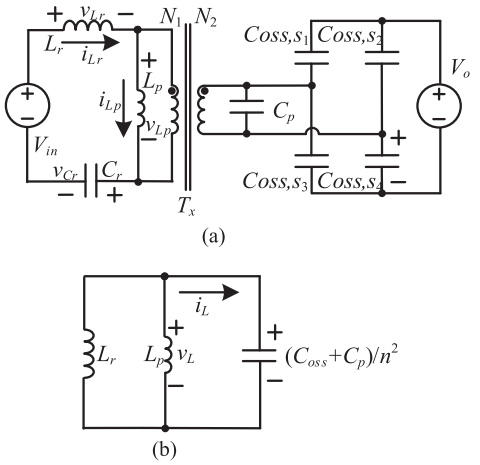

Fig. 8. Equivalent circuit of the *LLC* dc–dc converter during t_2–t_3. (a) Converter circuit during t_2–t_3. (b) Equivalent circuit.

The resonant angle frequency ω_h between (L_p//L_r) and C_e/n^2 is

$$\omega_h = \frac{1}{\sqrt{\frac{L_r L_p}{(L_r+L_p)}\frac{C_e}{n^2}}}. \tag{8}$$

According to KVL, the equation of the equivalent circuit in Fig. 8(b) satisfies

$$\frac{L_r L_p}{(L_r+L_p)}\frac{C_e}{n^2}\frac{d^2 v_L}{dt^2} + v_L = 0. \tag{9}$$

Then, the general solution of $V_{L,HF}$ (t–t_2) during t_2–t_3 can be obtained as

$$v_{L,HF}(t-t_2) = C_1 \cos\omega_h (t-t_2) + C_2 \sin\omega_h (t-t_2). \tag{10}$$

From (10), the general solution of $i_{L,HF}$ (t–t_2) is

$$\begin{aligned} i_{L,HF}(t-t_2) &= \frac{C_e}{n^2}\frac{dv_{L,HF}(t-t_2)}{dt} \\ &= \frac{\omega_h C_e}{n^2}\left[-C_1 \sin\omega_h (t-t_2) + C_2 \cos\omega_h (t-t_2)\right]. \end{aligned} \tag{11}$$

As the resonant capacitor voltage $v_{Cr}(t)$ and the resonant inductor current $i_{Lr}(t)$ are continued, it has

$$\begin{cases} v_{L,HF}(t_{2+}) = v_{L,HF}(t_{2-}) = nV_o - v_{L_p,LF}(t_2) \\ i_L(t_{2+}) = i_L(t_{2-}) = 0. \end{cases} \tag{12}$$

As the current flows from the primary side to the secondary side of the transformer is zero during O stage, the current $i_L(t_2)$ is zero. In addition, substituting (4) into (12), it has

$$\begin{cases} C_1 = nV_o - v_{L_p,O}(t_2) \\ \quad = nV_o + \frac{K}{K+1}\left(-2nV_o + V_{\text{in}} + \frac{V_o^2}{4C_r R_o V_{\text{in}} f_s}\right) \\ C_2 = 0. \end{cases} \tag{13}$$

Thus, the voltage $v_{L,HF}$ is

$$\begin{aligned} &v_{L,HF}(t-t_2) \\ &= \left[nV_o + \frac{K}{K+1}\left(-2nV_o + V_{\text{in}} + \frac{V_o^2}{4C_r R_o V_{\text{in}} f_s}\right)\right] \\ &\quad \cos\omega_h (t-t_2). \end{aligned} \tag{14}$$

As the voltage across switch S_2 and the voltage across switch S_3 are the same, the high-frequency component of the voltage $v_{ds,S2,HF}$ is

$$\begin{aligned} v_{ds,S2,HF}(t-t_2) &= \frac{v_{L,HF}/n}{2} \\ &= \left[\frac{V_o}{2} + \frac{K}{2n(K+1)}\left(-2nV_o + V_{\text{in}} + \frac{V_o^2}{4C_r R_o V_{\text{in}} f_s}\right)\right] \\ &\quad \times \cos\omega_h (t-t_2). \end{aligned} \tag{15}$$

Combining the high-frequency component analysis and the low-frequency component analysis, according to (6) and (15), the real voltage $v_{ds,S2}$ during t_2–t_3 can be obtained as

$$\begin{aligned} v_{ds,S2}(t-t_2) &= v_{ds,S2,LF}(t-t_2) + v_{ds,S2,HF}(t-t_2) \\ &= \frac{V_o}{2} - \frac{K}{2n(K+1)}\left[\begin{array}{l}\left(-2nV_o + V_{\text{in}} + \frac{V_o^2}{4C_r R_o V_{\text{in}} f_s}\right) \\ \quad \times \cos\omega_p (t-t_2) \\ + \frac{nV_o\pi\sqrt{K+1}}{2K}\sin\omega_p (t-t_2)\end{array}\right] \\ &\quad + \left[\frac{V_o}{2} + \frac{K}{2n(K+1)}\left(-2nV_o + V_{\text{in}} + \frac{V_o^2}{4C_r R_o V_{\text{in}} f_s}\right)\right] \\ &\quad \times \cos\omega_h (t-t_2). \end{aligned} \tag{16}$$

C. Simulated Verification

To verify the calculated results, a PSIM simulation is built. The following assumptions are made: the resonant components are $L_r = 20$ μH, $L_p = 220$ μH, and $C_r = 5$ nF, the switching frequency is 330 kHz, and the parasitic output capacitance of the SR switches $C_{oss,\text{SR}} = 1500$ pF. When the full-bridge *LLC* converter operates at 400 V input and 54 V output, Fig. 9(a) shows the simulated results and the theoretical results with the 10 A load current, and Fig. 9(b) shows the simulated results and the theoretical results with 20 A load current. The upper parts in Fig. 9(a) and (b) are the simulated results of the voltage $v_{ds,S2}$, and the voltages ringing during O stage are zoomed in and shown in the lower parts in Fig. 9(a) and (b), respectively.

From Fig. 9, the simulated results and the theoretical results are highly consistent, which verify the correctness of the theoretical analysis shown in (16). As can be seen from Fig. 9(a) and (b), along with the increasing load current, the voltage across the SR switch reaches zero during t_2–t_3. If the voltages across the SR switches are always higher than zero during t_2–t_3, the turn-ON early issue can be solved. Thus, an optimal design of the circuit parameters and the load conditions should be analyzed to solve the turn-ON early issue.

III. Optimal Design of the Circuit Parameters to Avoid the Turn-ON Early Issue of SR Switches

From (16), we can see that the voltage ringing across the SR switches depends on 12 variables, which are the output voltage V_o, the input voltage V_{in}, the magnetizing inductance L_p, the series resonant frequency f_r, the series resonant inductance

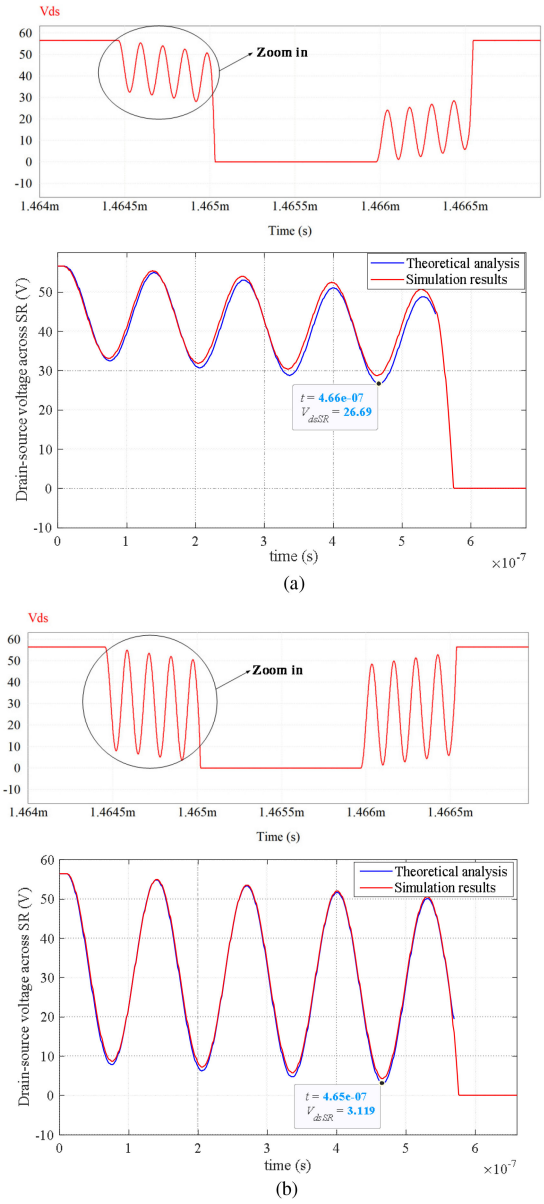

Fig. 9. Comparisons between the simulated results and the theoretical results of the voltage ringing during t_2–t_3. (a) With 10 A load current. (b) With 20 A load current.

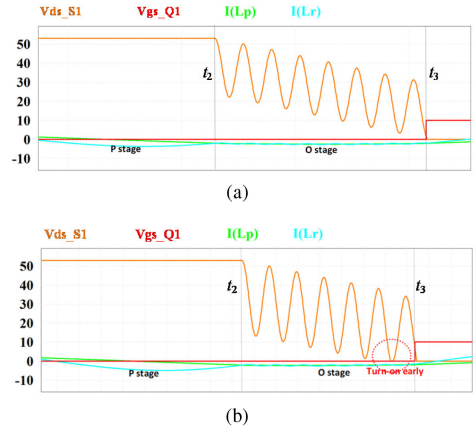

Fig. 10. First time t_{zero} that the drain-to-source voltage across SR switches reaches to zero during t_2–t_3. (a) $t_{\text{zero}} > t_3$. (b) $t_{\text{zero}} < t_3$.

L_r, the resonant capacitance C_r, the transformer turns ratio n, the parasitic output capacitance of the SR switches C_{oss}, the parasitic capacitance of the transformer C_p, the load resistance R_o, the switching frequency f_s, and the time t. Defining t_{zero} is the first time that the drain to the source voltage across SR switches reaches to zero during t_2–t_3. As shown in Fig. 10, the voltage ringing starts at the end of P stage t_2, and the O stage ends when the switch Q_1 is turned ON at t_3. When $t_{\text{zero}} > t_3$, the SR switches are not turned ON during t_2–t_3. When $t_{\text{zero}} < t_3$, the SR switches will be turned ON early by using the voltage sensing ICs.

Thus, to avoid the turn-ON early, the condition $t_{\text{zero}} > t_3$ is required by the optimal design of the circuit parameters. The objective function is

$$\begin{cases} t_{\text{zero}} > t_3 \approx \frac{1}{f_s} - \frac{1}{f_r} \\ t_{\text{zero}} = \min\left\{v_{ds,\text{SR2}}\,(t - t_2) = 0\right\}. \end{cases} \tag{17}$$

Considering that the range of some circuit parameters is narrow in industrial applications, we define some circuit parameters as constant to simplify the complexity. Taking the datacenter application as an example, assuming that the nominal output voltage $V_o = 54$ V, the series resonant frequency $f_r = 500$ kHz, and the transformer turns ratio $n = 8$.

As PO stage is usually considered as the major preferable operation stage, the PO stage is taken as an example in this article [8]. According to [14] and (2), the state equations of the *LLC* converter are

$$\begin{cases} I_{rPn}\sin(\theta_P + \theta_{P0}) = I_{rOn}\sin(\theta_{O0}) \\ -I_{rPn}\cos(\theta_P + \theta_{P0}) - 1 + \frac{1}{M} \\ \quad = -\sqrt{m}\cdot I_{rOn}\cos(\theta_{O0}) + \frac{1}{M} \\ I_{rPn}\sin(\theta_{P0}) = -I_{rOn}\sin\left(\frac{\theta_O}{\sqrt{m}} + \theta_{O0}\right) \\ -I_{rPn}\cos(\theta_{P0}) - 1 + \frac{1}{M} \\ \quad = \sqrt{m}\cdot I_{rOn}\cos\left(\frac{\theta_O}{\sqrt{m}} + \theta_{O0}\right) - \frac{1}{M} \\ I_{rPn}\sin(\theta_P + \theta_{P0}) = I_{rPn}\sin(\theta_{P0}) + \frac{\theta_p}{m-1} \\ p_{on}\frac{\pi}{f_s} = I_{rPn}\cos(\theta_{P0}) - I_{rPn}\cos(\theta_P + \theta_{P0}) \\ \qquad -I_{rPn}\sin(\theta_{P0})\theta_P - \frac{\theta_P^2}{2(m-1)} \\ \theta_P + \theta_O = \frac{\pi}{f_s} \\ m = (L_p + L_r)/L_r \end{cases} \tag{18}$$

where θ_P and θ_O represent the length of P and O stage, respectively, and P_{ON} is the normalized output power; I_{rPn} is the normalized magnitude of the current i_{Lr} in P stage, θ_{P0} is the initial phase angle of i_{rPn},; I_{rOn} is the normalized magnitude of the current i_{Lr} in O stage, and θ_{O0} is the initial phase angle.

From (18), as the voltage gain of the *LLC* converter can be derived by the resonant components' parameters L_r, L_p, and C_r, the switching frequency f_s, the transformer turns ratio n, and the load resistance R_o, the input voltage can be obtained by output

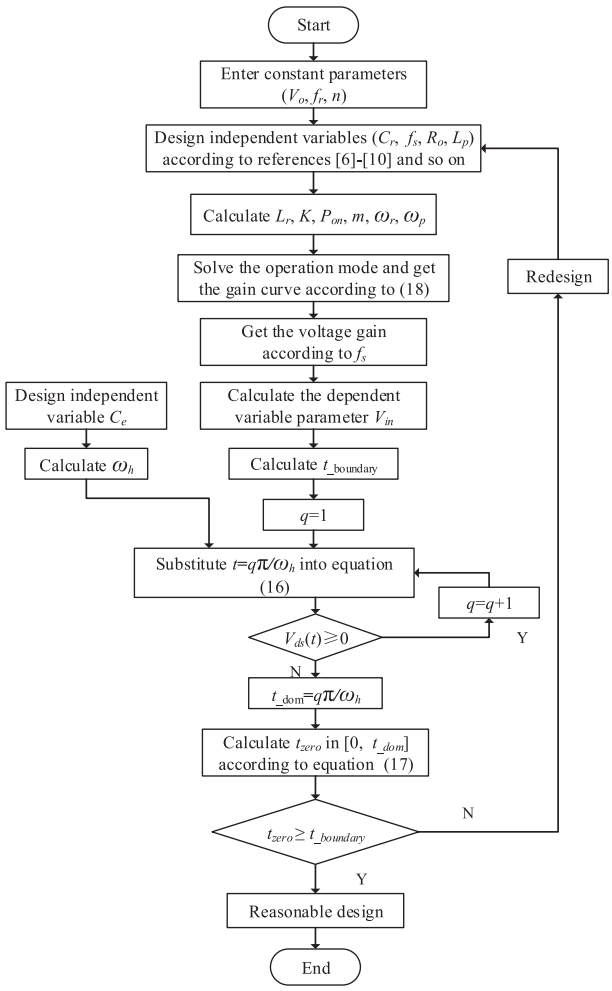

Fig. 11. Flowchart of the optimal design of the circuit parameters.

voltage and the voltage gain. Therefore, the input voltage $V_{\rm in}$ is not an independent variable.

The flowchart of the optimal design of the circuit parameters is shown in Fig. 11. Among the variables $V_{\rm in}$, V_o, L_p, L_r, C_r, C_e, R_o, n, f_r, and f_s, some circuit parameters are selected as constant to simplify the analysis, such as V_o, n, and f_r. Then, the variables L_p, C_r, C_e, R_o, and f_s can be designed according to [6]–[10] and so on. As the variable L_r can be obtained by C_r and f_r, and $V_{\rm in}$ can be obtained by L_p, C_r, L_r, R_o, V_o, n, and f_s according to (18), the $t_{\rm zero}$ only depends on the five independent variables L_p, C_r, C_e, R_o, and f_s.

Fig. 12 shows the relationship between the $t_{\rm zero}$ and the five independent variables. The area above the pink surface represents a safe area, which means $t_{\rm zero} > t_3$ and there is no turn-ON early issue; the area below the pink surface represents an unsafe area, which means $t_{\rm zero} < t_3$ and the SR switches will be turned ON early by using the voltage sensing method. Points A and B located above and below the pink surface are shown in Fig. 12. The two points are very close to the pink surface; thus, the accuracy of the voltage ringing model can be verified by the simulation results of the two points in Section IV.

From Fig. 12(b), (e), (f), and (h), the voltage ringing is more and more severe along with increasing load current I_o. From Fig. 12(a), (d), (e), and (g), the voltage ringing is more and more severe along with decreasing resonant capacitance C_r. From Fig. 12(a)–(c) and (j), the voltage ringing is more and more severe along with decreasing the switching frequency f_s/f_r. According to Fig. 12(c), (d), (f), and (i), and Fig. 12(g)–(j), the resonant inductance L_p and the parasitic capacitance C_e have a relatively small effect on the voltage ringing across SR switches.

In summary, when the circuit parameters of the *LLC* converter are designed by using the flowchart in Fig. 11, we can relieve the voltage ringing by decreasing load current, increasing resonant capacitance, or increasing switching frequency. From Fig. 11, if the designed circuit parameters satisfy the (17), the turn-ON early issue caused by the voltage ringing can be eliminated.

IV. Simulated Verification

A. Accuracy Verification

To verify the theoretical analysis, the PSIM simulation modes of the testing points in Fig. 12 are established. As there are ten A points and ten B points in Fig. 12, if 20 figures are given in this article, too many simulated waveforms will make confusion for the reader. Therefore, only the simulation waveforms corresponding to $t_{\rm zero}$ against C_r, R_o, and f_s in Fig. 12 are given in Fig. 13 because L_p and C_e have a relatively small effect on the voltage ringing across SR switches. The circuit parameters of testing points in Fig. 12(a), (b), and I are shown in Table I, and the simulation results of all the cases in Fig. 12 are given in Table II.

By using the circuit parameters, as shown in Table I, the PSIM simulation waveforms are shown in Fig. 13. From Fig. 13, although points A and B are very close, there is no turn-ON early issue in the simulation waveforms with all A points in Fig. 12(a), (b), and (e), and the SR switches are turned ON early in the simulation waveforms with all B points in Fig. 12(a), (b), and (e), which is consistent with the theoretical analysis.

To verify the accuracy of the theoretical analysis, the comparison between the calculated $t_{\rm zero}$ and the simulated $t_{\rm zero}$ is made in Table II. From Table II, the error between the calculation results in Fig. 12 and the simulation results in Fig. 12 is smaller than 0.43%, which shows that the theoretical model is very accurate. Therefore, by using the theoretical model to design the SR *LLC* converter with voltage sensing ICs, the turn-ON early caused by the voltage ringing will be eliminated.

B. Simulation Verification of the Designed Prototype

From the flowchart of the optimal design of the circuit parameters in Fig. 11, taking a prototype design as an example with 350–400 V input, 54 V output, and 20 A full load. According to [6]–[10] and the proposed design procedure and the voltage ringing across SR switches calculation model, the circuit resonant parameters $L_p = 165$ μH, $L_r = 23.2$ μH, $C_r = 5$ nF, and $n = 25{:}3$ are designed. Taking the circuit parameters and the parasitic capacitance $C_e = 7$ nF to (17), the testing point is located in the safe region in the calculation model. Fig. 14 shows

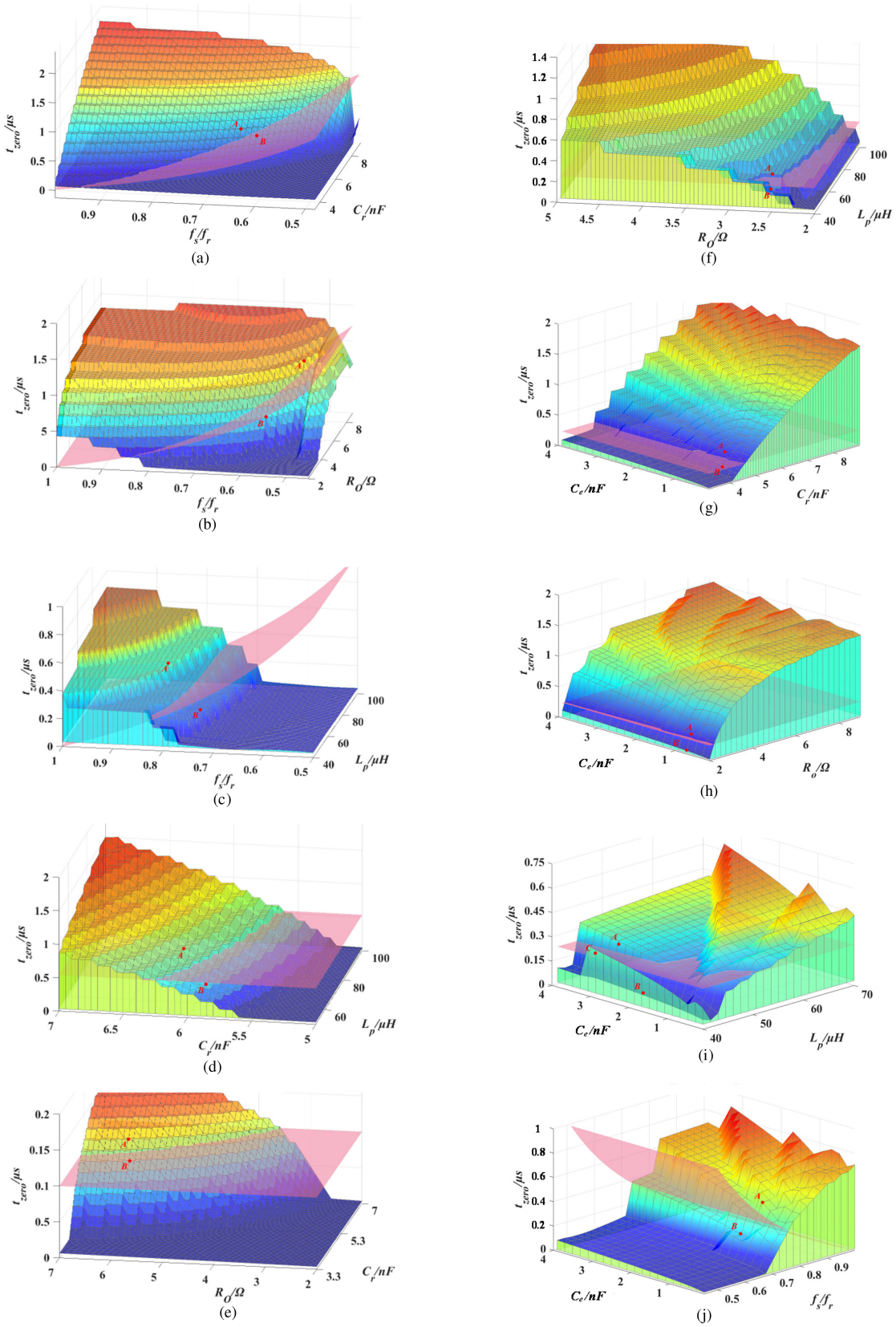

Fig. 12. Relationship between the t_{zero} and the independent variables. (a) *Cr* - *fs* - *t* (*Lp* = 100 μH, *Ro* = 2.43 Ω, and *Ce* = 1.5 nF). (b) *Ro* - *fs* - *t* (*Lp* = 100 μH, *Cr* = 5 nF, and *Ce* = 1.5 nF). (c) *Lp* - *fs* - *t* (*Ro* = 2.43 Ω, *Cr* = 5 nF, and *Ce* = 1.5 nF). (d) *Cr* - *Lp* - *t* (*Ro* = 2.43 Ω, *fs /fr* = 0.65, and *Ce* = 1.5 nF). (e) *Cr* - *Ro* - *t* (*Lp* = 100 μH, *fs /fr* = 0.5, and *Ce* = 1.5 nF). (f) *Lp* - *Ro* - *t* (*Cr* = 5 nF, *fs/fr* = 0.8, and *Ce* = 1.5 nF). (g) *Cr* - *Ce* - *t* (*Lp* = 100 μH, *Ro* = 2.43 Ω, and *fs/fr* = 0.8). (h) *Ro* - *Ce* - *t* (*Lp* = 100 μH, *Cr* = 5 nF, and *fs/fr* = 0.8). (i) *Lp* - *Ce* - *t* (*Ro* = 2.43 Ω, *Cr* = 5 nF, and *fs/fr* = 0.8). (j) *fs* - *Ce* - *t* (*Ro* = 2.43 Ω, *Cr* = 5 nF, and *Lp* = 100 μH).

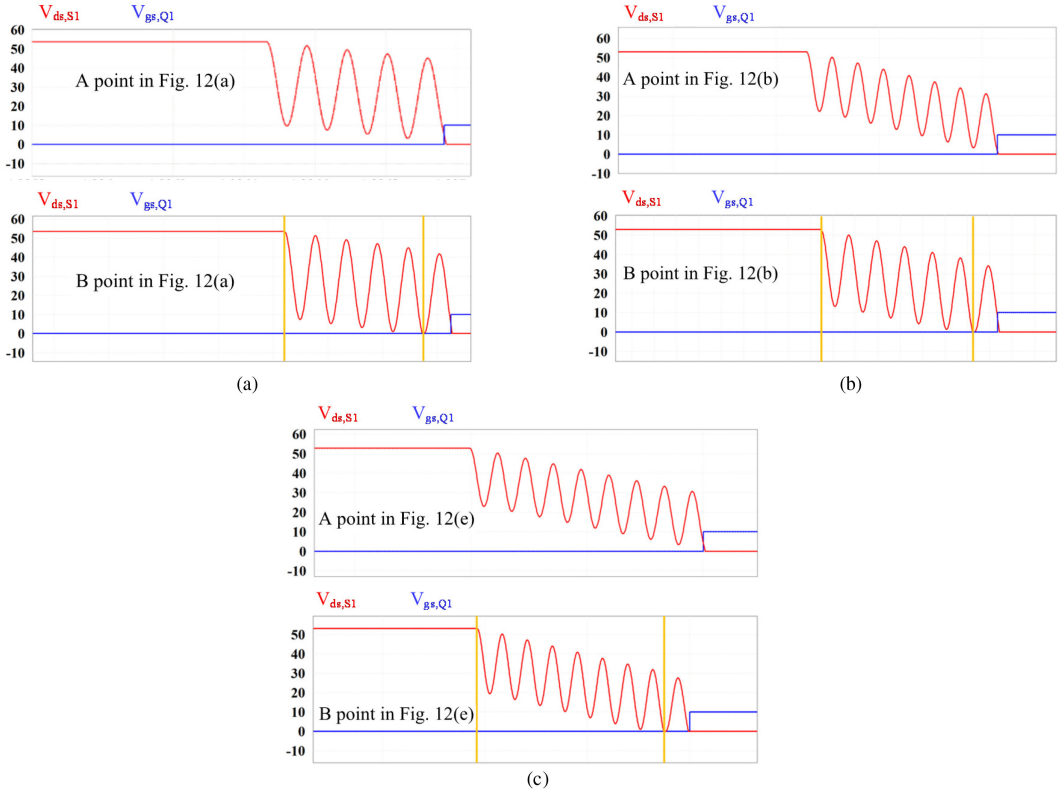

Fig. 13. PSIM simulation waveforms of the testing points in Fig. 12. (a) Simulated waveforms of the testing points in Fig. 12(a). (b) Simulated waveforms of the testing points in Fig. 12(b). (c) Simulated waveforms of the testing points in Fig. 12(e).

TABLE I
SIMULATED MODES OF THE TESTING POINTS OF FIG. 12

Test points \ Parameters		C_r (nF)	L_p (μH)	L_r (μH)	f_s/f_r	V_{in} (V)	V_o (V)	I_o (A)	C_e (nF)
C_r - f_s - t	A (safe)	6.2	100	16.342	0.67	343.5420	54	22.2222	1.5
	B (unsafe)	6.3	100	16.083	0.63	327.7279	54	22.2222	1.5
R_o - f_s - t	A (safe)	5.0	100	20.264	0.52	204.7871	54	8.4375	1.5
	B (unsafe)	5.0	100	20.264	0.57	256.9875	54	12.8571	1.5
C_r - R_o - t	A (safe)	5.5	100	18.422	0.50	205.1445	54	8.8525	1.5
	B (unsafe)	5.2	100	19.485	0.50	195.3497	54	9.0000	1.5

the PSIM simulation waveforms of SR switches with 20 A load at 400 V input and 14 A load at 350 V input by using the designed circuit parameters. From Fig. 14, the load current is increased to 20 A at 400 V input, and the minimum value of the voltage ringing across SR switches is around 6 V. It can be seen that the drain–source voltages of SR switches are higher than zero during O stage, and the SR controller can generate the correct driving signal. From Fig. 14(b), the measured resonant period of the voltage ringing is 289 ns. Taking the circuit parameters and the parasitic capacitance $C_e = 7$ nF to (8), the calculated resonant period of the voltage ringing is 284 ns, which is consistent with the measured value and verifies the correction and accuracy of the theoretical analysis.

By using the voltage sensing SR control strategy, this article can provide a design guideline for the high-load-current and high-output-power *LLC* converter.

V. EXPERIMENTAL RESULTS

From the aforementioned analysis and simulated results, a two-phase interleaved *LLC* dc–dc converter is designed to verify the theoretical analysis, which consists of two paralleled *LLC* converters, as shown in Fig. 1, with 20 A rated load current for each phase. A 2.16-kW prototype with 350–400 V input and 54 V output is built according to the proposed guideline of the circuit parameters design. In the proposed prototype, the rated output current of one phase is 20 A when the input voltage is 400 V, while the output current of one phase is 70%×20 A = 14 A when the input voltage is lower than 400 V rated input voltage. The specification and circuit parameters of the converter are shown in Table III, and the two-phase interleaved waveforms are shown in Figs. 15(b), 16, and 17.

Fig. 15(a) shows the ZVS turn-ON of switch Q_1 in the phase 1 circuit, and Fig. 15(b) shows the transformer secondary currents

TABLE II
SIMULATED MODELS OF THE TESTING POINTS IN FIG. 12

Results / Test points		Calculation results $t_{zero}(\mu s)$	Simulation results $t_{zero}(\mu s)$	Error
C_r - f_s - t	B point	0.5033	0.5037	0.079%
R_o - f_s - t	B point	0.6778	0.6766	0.177%
L_p - f_s - t	B point	0.1669	0.1669	0.000%
C_r - L_p - t	B point	0.3618	0.3614	0.110%
C_r - R_o - t	B point	0.9124	0.9129	0.055%
L_p - R_o - t	B point	0.0555	0.0556	0.179%
C_r – C_e - t	B point	0.1560	0.1561	0.064%
R_o – C_e - t	B point	0.1866	0.1868	0.107%
L_p – C_e - t	B point	0.8924	0.8924	0.000%
f_s – C_e - t	B point	0.2100	0.2109	0.427%

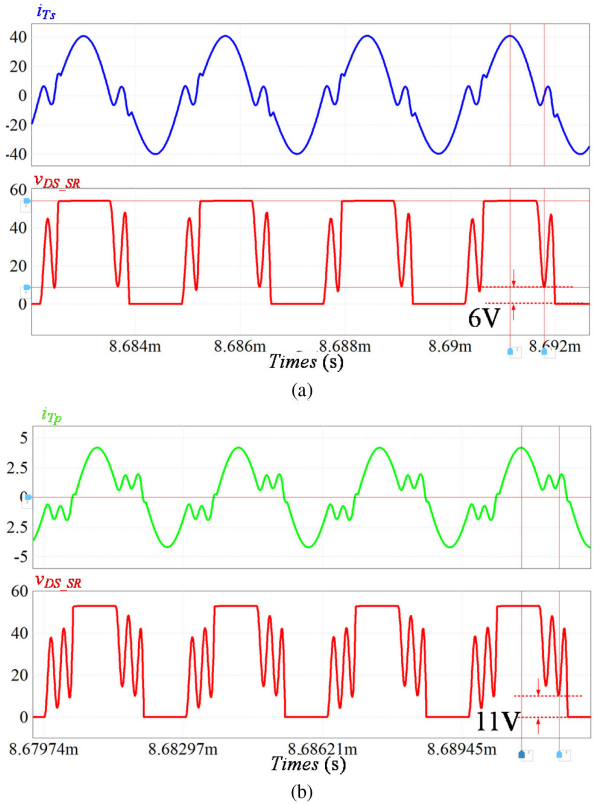

Fig. 14. Simulation waveforms of the designed *LLC* converter at (a) 400 V input, 54 V and 20 A output, and (b) 350 V input, 54 V and 14 A output.

TABLE III
SPECIFICATIONS AND PARAMETERS OF THE PROPOSED *LLC* CONVERTER

System Specification	
Input voltage	350 V – 400 V
Output voltage	54 V
Rated output current	20 A×2 for two-phase converter (400 V input)
Rated output power	1080 W×2=2160 W
Circuit Parameter	
Transformer	N = 25/3, PQ35/35 core, 3C97 material
Magnetizing inductor (L_m)	165μH integrated in the transformer
Series inductor (L_r)	23.2 μH, PQ32/20 core, 3C97 material
Series capacitor (C_r)	5 nF
Parasitic capacitance (C_e)	$C_{oss,\ SR}$=4.9 nF (V_{DS}=54 V) C_p= C_e−$C_{oss,\ SR}$=7.1 nF−4.9 nF =2.2 nF
Primary-side switches	GPI65010DF56 (650 V, 10 A) × 4
Secondary-side switches	IPT012N08N5 (80 V, 300 A) × 4
Output capacitor	C3225X7R1N106K250AC, 250 V, 10 μF × 9 + 470 μF E-cap
Microcontroller	dsPIC33EP16GS506

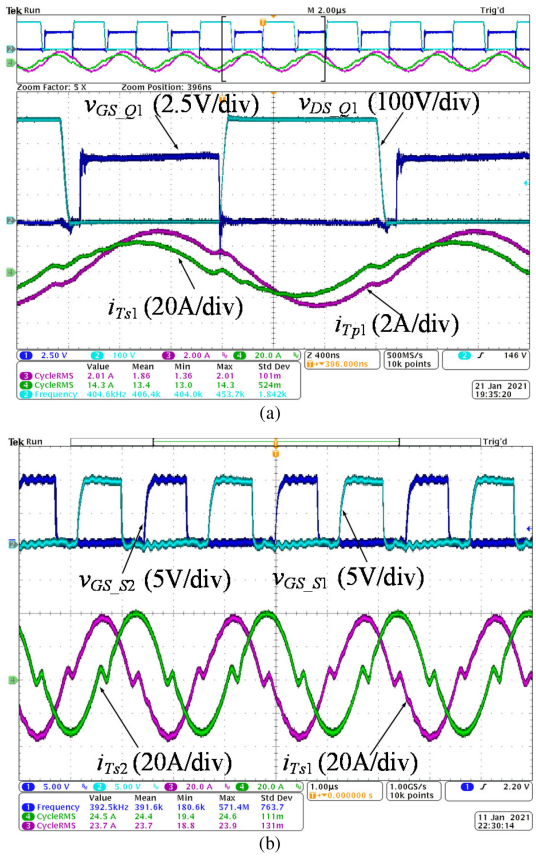

Fig. 15. Experimental waveforms of the designed *LLC* converter at (a) 400 V input, 54 V output, and 7.5 A load current for each phase and (b) 400 V input, 54 V output, and 20 A load current for each phase.

in phase 1 and phase 2. As shown in Fig. 15(b), by using the voltage sensing IC NCP4305, the SR gate driving signals are generated for switches S_1 and S_2 in the phase 1 circuit, which keeps the transformer secondary currents flowing through SR switches to reduce the conduction loss. The gate signals of transformer primary switches are shown in Fig. 15(a), and the gate signals of transformer secondary switches are shown in Fig. 15(b). From Fig. 15(b), the SR switches are turned ON properly, and there is no turn-ON early issue at full load.

From Fig. 12(b), (e), (f), and (h), the voltage ringing is more and more severe along with increasing load current I_o. Thus, the experimental waveforms under the rated load current are shown in Fig. 16(b). Although only 70% rated load current is provided when the input voltage is lower than 400 V, switching

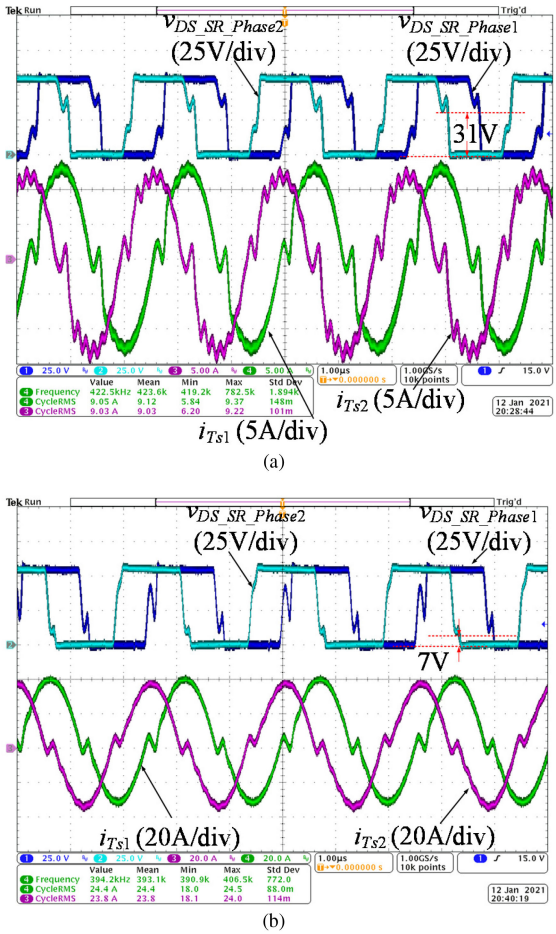

Fig. 16. Experimental waveforms of the designed *LLC* converter at (a) 400 V input, 54 V output, and 7.5 A load current for each phase, and (b) 400 V input, 54 V output, and 20 A load current for each phase.

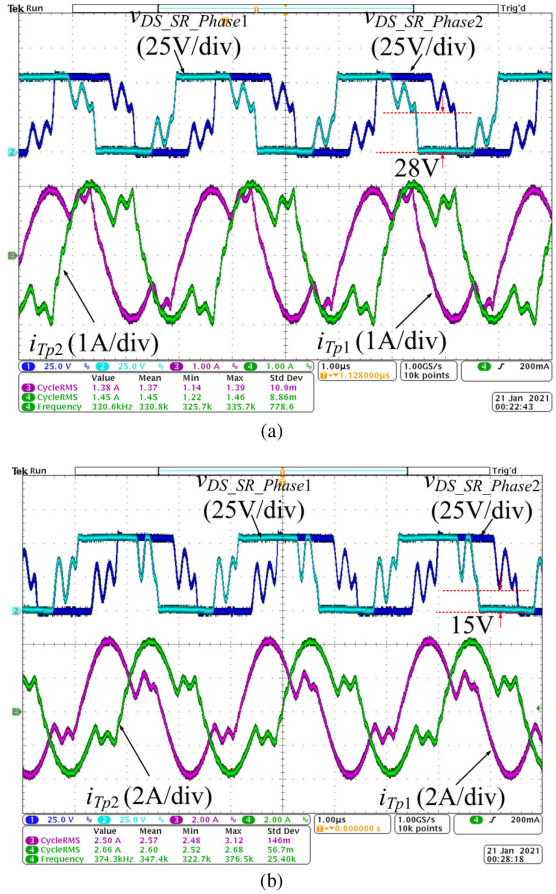

Fig. 17. Experimental waveforms of the designed *LLC* converter at (a) 350 V input, 54 V output, and 7.5 A load current for each phase, and (b) 350 V input, 54 V output, and 14 A load current for each phase.

frequency f_s is lower to increase voltage gain to keep 54 V output. From Fig. 12(a)–(c) and (j), the voltage ringing is more and more severe along with decreasing the switching frequency f_s/f_r. Therefore, the experimental waveforms under 70% rated load current and 350 V input are shown in Fig. 17(b) to judge which is the worst case for the voltage ringing in the proposed prototype.

Fig. 16 shows the drain-to-source voltages across the SR switches and the transformer secondary currents of phase 1 and phase 2 circuits at 400 V input and 54 V output. As shown in Fig. 16, along with the load-current increment from 7.5 to 20 A, the minimum value of the voltage ringing across SR switches is changed from 31 to 7 V, which verifies the analysis in which the voltage ringing is more and more severe along with increasing load current. According to Fig. 16, if the load current is increased further, the voltage ringing would reach to zero and the converter operates at unsafe region. By substituting the circuit parameters in [10] and [34] to (17), the calculation results show the converters operate at unsafe region, which are consistent with the experimental results of the safe region and unsafe region in [10] and [34].

Fig. 17 shows the drain-to-source voltages across the SR switches and the transformer primary-side currents of the two-phase *LLC* converters at 350 V input and 54 V output. When the load current is 7.5 A and 14 A load current for each phase, the minimum values of the v_{ds} are 28 V and 15 V, respectively. From Fig. 16(a) and 17(a), at the same load current, the minimum value of the voltage ringing across SR switches is changed from 31 to 28 V when the switching frequency is changed from 423 to 331 kHz, which verifies the analysis in which the voltage ringing is more and more severe along with decreasing switching frequency.

From Figs. 16 and 17, the load resistance R_o has a larger effect than the switching frequency f_s on the voltage ringing across SR switches. Therefore, the worst condition of the proposed prototype for the voltage ringing is 400 V input and 20 A load current. From Figs. 16(b) and 17(b), the experimental results are consistent with the simulated results in Fig. 14, which verifies the correctness and effectiveness of the analysis.

As shown in the experimental results in Fig. 17(b), the resonant period of the voltage ringing is measured as 287 ns, and thus, C_e is 7.1 nF in the prototype according to (8). From the datasheet of the SR switches, the equivalent output capacitance $C_{oss,\,\mathrm{SR}}$ is around 4.9 nF when the output voltage is 54 V. Therefore, we can

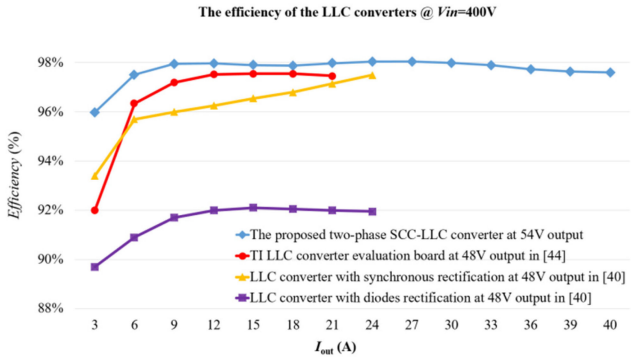

Fig. 18. Efficiency comparison between the designed *LLC* converter and the previous works.

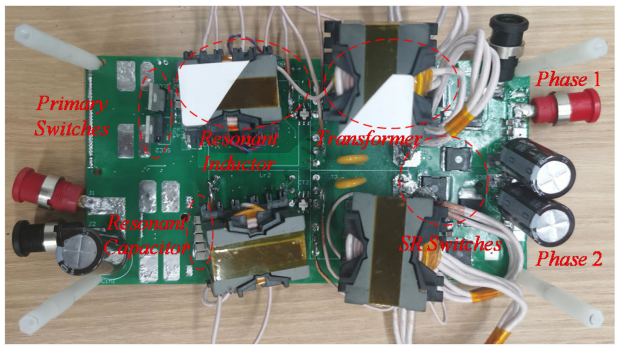

Fig. 19. Prototype of the *LLC* converter.

calculate that the transformer secondary parasitic capacitance C_p is 2.2 nF.

At light load, the current ringing, as shown in Figs. 16(a) and 17(a), is caused by the parasitic parameters, such as the parasitic capacitance of the series resonant inductor, the parasitic capacitance of the transformer, and the leakage inductance of the transformer. At high load, the current ringing is not obvious in Figs. 16(b) and 17(b). As the severe voltage ringing generally occurs at high load instead of light load, these parasitic parameters are not analyzed in this article to simplify the complexity of the voltage ringing model.

As the circuit parameters C_r, L_p, C_e, etc., have a tolerance between the two circuits, the two-phase waveforms are not very the same exactly. As the difference between the two-phase waveforms is small and the theoretical analysis in this article can be verified by Figs. 15–17, the tolerance is neglected in this article.

In the designed *LLC* converter, phase shedding technology is adopted to improve light-load efficiency, and a 20 A load current is provided by each phase at full load. The blue line in Fig. 18 shows the measured efficiency of the designed two-phase *LLC* dc–dc converter. By using the voltage sensing SR controller and the circuit parameters according to the proposed design guideline, the peak efficiency of the prototype reaches 98.1%, and the full load efficiency is 97.6%. In Fig. 18, the efficiency of the prototype is compared between this work and the previous works with a similar specification. The red and yellow lines represent the measured efficiency of the *LLC* converter with SR in [44] and [40], and the purple line represents the measured efficiency of the *LLC* converter with diodes rectification in [40]. From Fig. 18, the efficiency of the proposed prototype is high, which verifies the effectiveness of the proposed design principle of the *LLC* converter. Fig. 19 shows the prototype of the *LLC* converter.

VI. Conclusion

Voltage sensing SR control strategy is used widely in high-load-current *LLC* dc–dc converter in industrial applications. This article presents the accurate analysis and design of the circuit parameters of SR *LLC* dc–dc converter, which can avoid voltage ringing across SR switches reaches to zero and make voltage sensing SR controller generate false driving pulses. By using the proposed parameters design principle and the voltage ringing across SR switches calculation model, the SR switches turn-ON early issue or the SR switches turn-ON several times in one cycle issue is eliminated, which guarantees that the voltage sensing SR ICs work well. Therefore, the proposed analysis of the voltage ringing across SR switches and the parameters design principle can provide a reference and guideline for the high-load-current and high-output-power *LLC* converter with the voltage sensing SR control strategy.

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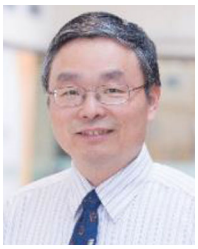

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