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A Discussion on Ultra-High Efficiency and Ultra-High Power Density DC-DC Converter Technologies

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***Abstract*—This paper discusses the challenges in achieving ultra-high efficiency, defined here as higher than 99% efficiency, as well as high power density of more than 2kW/in^3 for DC-DC converters. For simplicity, our discussion focuses on 48V to 12V converters aimed primarily at data center applications, but the concepts discussed are broadly applicable to DC-DC conversion at a wide range of voltage levels. This paper will present a review of the fundamental sources of losses in DC-DC converters and how to minimize them, as well as a more in-depth look at some of the most efficient and dense topologies presented in literature thus far.**

Based on this analysis and review the key concepts that enable DC-DC converters to achieve higher than 99% efficiency at a power density of more than 2kW/in^3 will be summarized which include: easily paralleled "modular" designs to reduce conduction loss, multi-level structures that reduce individual component voltage stresses, utilizing lower switching frequencies to reduce switching and quiescent losses, operating with full duty ratio to ensure maximum utilization of the power components, and utilizing novel circuit topologies that nearly eliminate bulky, lossy magnetic components when compared with conventional topologies.

***Index Terms*—DC-DC Converter, Ultra-High Efficiency, 99% Efficiency, Ultra-High power density, Full duty ratio**

I. Introduction

As device technology improves and new circuit topologies are developed, designers and engineers are targeting increasingly ambitious values for efficiency and power density. With conventional topologies, such as a Buck converter, efficiencies above 99% are not practical to achieve. However, several circuit topologies have been developed in recent years that have demonstrated this ultra-high efficiency level in laboratory conditions. This paper will present a review and discussion of some of these topologies, discussing some of the key commonalities that have been developed to enable these groundbreaking efficiency levels. The topologies discussed in detail in this paper will primarily be focused on DC-DC converters targeting 48V to 12V conversion, as this has become a very active and competitive research area in recent years, in particular for data center applications. The key concepts presented for achieving ultra-high efficiency, defined here as 99% efficiency or higher, are applicable to a wide range of different voltage and current levels, however.

In addition to high efficiency, a consideration of equal, or perhaps greater, importance in certain applications is the power density achieved by these circuit topologies. Ultra-high efficiency topologies have several inherent benefits that can allow for higher power density levels than might be possible with conventional circuit designs. By operating at such high efficiency levels, the thermal performance of the converter is greatly improved. This allows higher power levels to be delivered within the same volume. Additionally, as will be discussed in greater detail in this paper, many ultra-high efficiency topologies greatly reduce their reliance on magnetic components and reduce the voltage and current stress of individual circuit components. Magnetic components are typically one of the bulkiest components in a Buck converter, and eliminating, or greatly reducing, the inductance required provides significant improvements in terms of overall converter size.

The chart shown below in Fig. 1 shows a collection of designs for 48V to 12V conversion. These converter designs can be broadly categorized as (1) Isolated Regulated topologies, (2) Non-isolated Regulated topologies, and (3) Non-isolated Unregulated topologies.

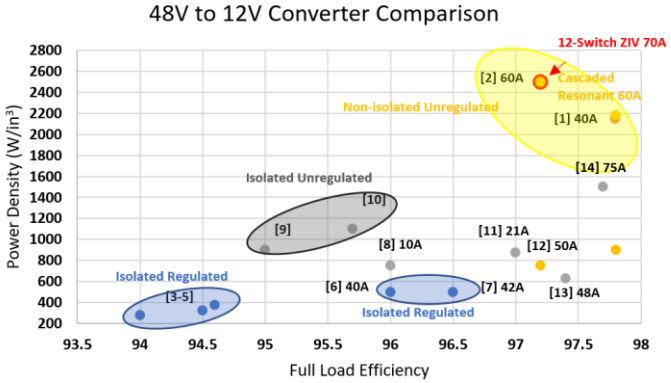

Fig. 1. A comparison of efficiency and power density achieved by various 48V to 12V DC-DC converters referenced from [15]

This chart shows a clear trend, wherein Non-isolated Unregulated topologies offer huge gains in terms of both efficiency and power density. It follows then that the majority of topologies that have demonstrated ultra-high efficiency of more than 99% fall into this category. However, eliminating both isolation and regulation does limit the number of

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applications that these topologies can be used in. Speaking broadly, these ultra-high efficiency converters are most often proposed for use as so-called intermediate bus converters, as part of a multi-stage power conversion solution where a large step-down ratio is required but high efficiency is desired. One very common target for this is 48V to 12V conversion in data centers, hence the large number of topologies presented in Fig. 1. In these applications the bus converter operates as a sort of "DC-DC transformer" or "DC-X" module, reducing the input voltage to the Point-of-Load (POL) converter which will provide regulation for the load.

It is a common myth that a two-stage conversion process, such as one using an intermediate bus converter, has inherently higher losses than performing the conversion in a single step. In particular with the advent of these ultra-high efficiency and high power density circuit topologies this is now far from the truth. As the input voltage increases and large step-down ratios are required, the challenges of a single-step conversion only increase further. By contrast, when considering ultra-high efficiency topologies that can operate with up to 99% efficiency, the reduction of input voltage for the POL converter, and corresponding size/efficiency improvements this enables, will be more than enough to increase the overall system efficiency when compared with a single-stage power delivery solution.

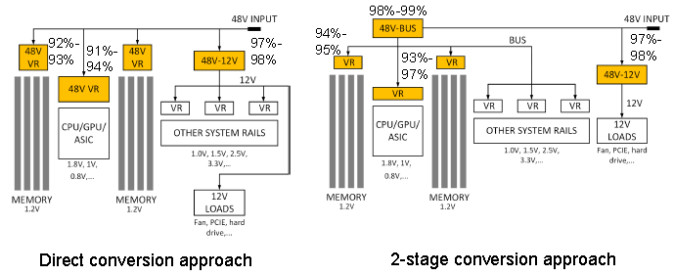

Fig. 2. A comparison of direct conversion and 2-stage conversion approach referenced from [16]

Fig. 2 presents a diagram referenced from [16] presented by Google as part of their discussion to move to a 48V architecture in their data centers. Of note here is that when a 98%-99% bus converter is utilized, the POL converter that is responsible for converting 48V down to less than 1V must be 91%-94% efficient to be competitive with a 2-stage conversion approach. Even considering a 12V to 1V multi-phase Buck converter design for GPU applications using sophisticated Smart Power Stage components [17-18] can only achieve 87% efficiency (using a typical full-load value of 50A/phase), with a peak efficiency at light load of 92%. Increasing the input voltage to 48V will significantly reduce these efficiency levels even further.

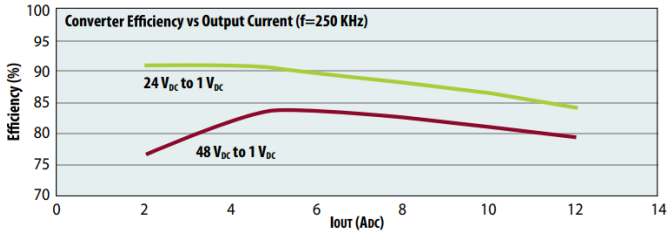

Fig. 3. 48V to 1V vs 24V to 1V Efficiency with Buck Converter [19]

As a second example the EPC1001/1007 evaluation circuit can be examined [19]. This circuit uses the exact same design for both 24V/1V conversion and 48V/1V conversion. For the same output power, doubling the input voltage will decrease the peak efficiency from 90% to 82% and full load efficiency from 84% to 79%. Furthermore, this reduction in efficiency does not even consider the performance improvements that could be achieved by utilizing lower voltage FETs in the two-stage solution.

In summary, there is a clear need for an ultra-high efficiency and extremely high density bus converter in order to enable higher bus voltages and support the ever-increasing power demands in highly innovative sectors such as data centers, servers, and high-performance computing. One of the key goals of this paper is to examine the common features of these bus converter topologies and the design concepts that allow them to achieve efficiencies above 99% and power densities of more than 2kW/in^3 for 48V to 12V conversion.

II. Achieving Ultra-High Efficiency and Power Density

This section will present some of the key design concepts / considerations that, when combined, can enable ultra-high efficiency and high-density bus converter topologies. As will be shown in Section III, the existing topologies in literature take advantage of many, or even all, of these key concepts to achieve extremely high efficiency and power density.

A. Optimizing Conduction Losses

The conduction loss in a converter is very straightforward to calculate and represents a fundamental efficiency limit for a given topology.

$$P_{cond} = I^2 R_{eq} \tag{1}$$

The conduction loss simply depends on the square of the current, and the equivalent resistance. From this perspective, there are far fewer "knobs" a designer can utilize to reduce or design around the conduction losses in a converter, as compared to something like the switching losses. In ultra-high efficiency applications, the conduction loss will typically be the dominant source of loss in the converter, particularly as load currents increase. This means that an ultra-high efficiency topology should have a few key characteristics to minimize the overall conduction loss as much as possible. The R_{eq} parameter depends on the components used in the converter topology itself. Sources of this equivalent resistance include switches, series capacitors (used in many switched capacitor topologies), inductors and PCB traces/wires.

For a given R_{eq} the only way a designer can further reduce the conduction loss of a converter is by reducing the current stress of the components. One very important technique to achieve this is through multi-phase operation. By dividing the load current across multiple phases, the overall conduction loss can be greatly reduced. In addition, with multi-phase operation it is often possible to achieve interleaving which further reduces the current stress of input and output capacitor components. Thus, the ability to parallel multiple phases easily is extremely

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desirable as it is one of the very few options a designer has to reduce the conduction losses and handle higher current levels.

The other possible approach is reduction of R_{eq} itself. In terms of switches, the technology behind these devices is constantly improving and significant performance gains are achieved year over year as new devices are developed. It remains to be seen whether this improvement will eventually stagnate, but even as recently as 2021 companies such as Infineon have released new generation MOSFETs with on-state resistances that nearly half of the previous generation for the same voltage rating, package size, and also similar gate charge.

Table 1. Comparison of Figure of Merit between selected current and previous generation MOSFETs

Parameter	BSZ025N04LS	BSZ021N04LS6	IQE013N04LM6
Vds (V)	40	40	40
Rds(on) (mΩ)	2.5	2.1	1.35
Qg (nC)	37	31	41
FOM	92.5	65.1	55.35

The key takeaway from this is that circuit topologies that rely on larger numbers of switches while reducing the passive components (capacitors, inductors) needed may have an advantage, especially looking forward to the future as active devices continue to improve with new technologies.

B. Optimizing Switching Losses

The switching loss in a converter represents another dominant source of loss that must be reduced in order to achieve ultra-high efficiency.

$$P_{sw} = \frac{1}{2} VI\left(t_{on} + t_{off}\right) f_{sw} \quad (2)$$

The switching loss is more complex than conduction loss, and depends on more factors; however, this gives designers more options to optimize and reduce the switching loss.

The previous discussion on the improvement of MOSFET technologies and the impact on conduction loss also applies to switching losses. The Figure-of-Merit (FOM) is presented as the product of the $R_{ds(on)}$ and Q_g of a switching device, intended to give a single number representing the "lossiness" of the switch, with lower FOM values indicating higher performance. As shown in Table 1 above, the latest generation of MOSFETs have a FOM that is greatly improved from the previous generation of parts. However, these improvements are achieved even when considering only traditional silicon MOSFETs. Wide bandgap materials such as GaN (Gallium Nitride) will also allow for further improvements in switching performance. In the past, papers such as [20] have shown that for low voltage, GaN devices offered relatively little gain over the silicon devices available. However, as companies such as EPC have continued to expand their portfolio of devices it has become clear that GaN can offer significant performance gains at low voltage levels as well. Based on these new products, such as the EPC2069, the previous analysis was limited simply by the relatively small number of products available and GaN still had "untapped potential" at that time.

Table 2. Comparison of Figure of Merit between selected silicon MOSFET and GaNFET devices

Parameter	EPC2069 (GaN)	BSZ021N04LS6	IQE013N04LM6
Vds (V)	40	40	40
Rds(on) (mΩ)	1.6	2.1	1.35
Qg (nC)	12.5	31	41
FOM	20	65.1	55.35

As shown in Table 2, the FOM for the GaN device is less than half of even the new generation silicon MOSFETs, and this is largely driven by the extremely low Q_g value of the GaNFET. This small Q_g reduces the t_{on} and t_{off} values for the switch, and significantly reduces the switching loss through this.

New switching devices reduce the switching time and therefore, reduce the switching loss. Once again this reinforces the idea that with the advances of switching devices, that circuit topologies that are able to "trade" inductors and capacitors for switching devices may offer better performance.

As shown in (2), the switching loss can also be reduced by lowering the voltage and current stress of the switching device. Unfortunately, while multi-phase parallel operation can reduce the conduction loss, it cannot reduce the overall switching loss. This is because while the current stress is decreased, the number of switching devices is increased.

The voltage across the switching devices, however, can be reduced through a multilevel structure which is used in many switched capacitor converters. In these structures, flying capacitors reduce the voltage stress of the individual switching devices, usually by a factor of ½ or more. The FOM for a MOSFET depends strongly on the voltage rating of the device [21].

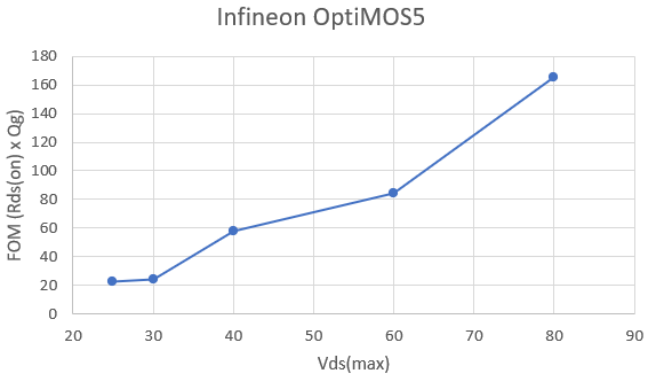

Fig. 4. Example FOM for OptiMOS5 Parts in SuperSo8 packaging

Using the example above from devices selected from the OptiMOS5 family of parts, for the same packaging, if a 30V device can be used in place of a 60V device, then the FOM can be reduced by a factor of 4 (a reduction from 80 to 20)

Therefore, a multilevel structure that reduces the voltage stress of the switching devices can greatly reduce the switching losses in a converter by not only reducing the voltage across the switch directly, but also by enabling higher FOM devices to be used. As discussed in the previous section enabling higher FOM

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devices to be used may also have benefits in terms of conduction losses.

Another well-known, but often neglected approach to reduce the switching loss is to reduce the switching frequency. Reducing the switching frequency by half will reduce the switching loss by half, while also reducing other frequency dependent losses such as the gate drive loss. From an efficiency perspective this is very desirable, but in many converter topologies this is not possible as it increases the size of capacitive and magnetic elements. Magnetic components are often the bulkiest and lossiest components in many converter topologies. Therefore, with the goal of achieving more than 99% efficiency and high power density, a designer is presented with two conflicting ideas. First, it is desirable to minimize the magnetic components required. Second, it is desirable to keep the switching frequency low to minimize losses.

C. Magnetics Size Reduction

Inductors and magnetics typically represent one of the largest and lossiest components in a conventional power converter design. When a large inductor is required, such as in a Buck converter, the DCR of the inductor can be significantly larger than that of the switches and dominate the overall conduction loss of the converter, even while neglecting additional magnetics related losses such as the core loss.

The size of the inductor is typically determined by the acceptable ripple current, which depends on the volt-second applied to the inductor. Increasing the switching frequency reduces the "second" component of this, allowing for smaller magnetics to be used. As discussed previously, however, from an efficiency perspective it is desirable to operate at a low switching frequency.

A hallmark of many ultra-high efficiency and density topologies that will be discussed in the next section is the huge reduction in inductance value required through the reduction of the "volt" component of the volt-second product. In many of these topologies, so-called "full duty-ratio" topologies, the inductor sees almost no voltage across it throughout a switching cycle [22-23]. The overall inductance value needed in these converters can be more than 100x less for the same ripple. In some topologies this is because the half-resonant corner frequency is at the switching frequency, rather than at around $1/10^{th}$ of the switching frequency in a traditional PWM converter. Furthermore, when using half-resonant techniques, the volt-second of the resonant inductor is typically about $1/4^{th}$ of that in a traditional PWM converter.

Minimizing the inductor size is one of the key enablers of ultra-high efficiency and power density as the magnetic components required in conventional PWM converters are typically the largest and lossiest component in the circuit design.

Additionally, this full duty ratio, also discussed in [24] represents maximum utilization of the converter devices. Operating at less than full duty ratio necessarily means that some devices, whether they be switches or capacitors, are not fully utilized and the power density of the converter will be significantly lower than in a comparably designed full duty ratio converter.

Typically, in these full-duty ratio converters, more capacitors are required. As capacitors have an energy/power density that can be orders of magnitude higher than inductors, utilizing capacitors to do the bulk of the energy storage in a DC-DC converter topology becomes a very attractive option. We can even go as far as to say that to achieve ultra-high efficiency and power density, it is desirable to use more silicon (or GaN) and capacitors in order to reduce magnetics.

Similar to the conduction loss, the inductor losses can be greatly reduced through multi-phase operation by reducing the current carried by each individual inductor. Interleaving can also be achieved by some topologies on the output inductors, further reducing the inductance value (and by extension the size) required.

D. Features of Ultra-High Efficiency Topologies

Resonant converters [25-29] utilize the addition of inductive and capacitive elements to create sinusoidal currents or voltages within the converter. A resonant converter can be designed such that at the time of switching, the current flowing through, or voltage across, a switching device is zero (or nearly zero). This theoretically eliminates the power loss associated with the turn-on and/or turn-off of the switching device. While eliminating the turn-on and turn-off losses is of a huge benefit in terms of efficiency, the design of the resonant components can be challenging, requiring precise values.

Additionally, like in a Buck converter, it is desirable to operate at higher frequencies to reduce the size of these resonant components. Other frequency related losses, such as driver losses, cannot be eliminated by resonant operation and thus operating at higher frequencies still presents a drawback to achieving ultra-high efficiency. Most resonant converters also cannot be easily paralleled, which is one of the few ways that conduction losses can be lowered for a given power level, making their design somewhat inflexible. In addition to the inability to easily parallel multiple phases, the resonant current of the converter increases the RMS current stress seen by the devices, increasing conduction losses. Due to these drawbacks resonant operation is therefore not a "magic bullet" to enable ultra-high efficiency.

While topologies such as resonant converters and buck converters must operate at higher switching frequencies in order to minimize the size of the magnetic components in the converter, novel ultra-high efficiency topologies are able to minimize the size of their magnetic components through the converter topology itself.

By reducing the voltage applied to the inductor over one switching period, the required inductance value can be significantly reduced. This can be achieved by relying more

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heavily on capacitors instead of inductors for energy storage. In these topologies the inductance value can be reduced by more than 100 times.

In addition to the inherent benefits of eliminating large and lossy magnetic components, this allows for these converter topologies to operate at much lower switching frequencies (less than 200kHz) without paying a significant size penalty. By operating at lower frequencies, the switching losses are further reduced, and losses such as the gate drive loss that can dominate at very light load (and are not eliminated by resonant operation) are also reduced. Operating at low switching frequency is therefore very desirable from an efficiency perspective, and as will be shown in the next section, some novel circuit topologies are able to operate at low switching frequency while maintaining extremely high power density by eliminating magnetic components.

In summary, there are a few critical techniques that have been demonstrated in literature that can allow for 99% efficiency to be achieved while maintaining very high power density. These same commonalities appear in different topologies presented by different research groups, and the majority of the ultra-high efficiency topologies currently presented in literature use several (or even all) of these techniques.

- Easily Paralleled Design
- Multi-Level Structure
- Low Switching Frequency
- Full Duty Ratio
- Near Elimination of Magnetics (100x reduction)

III. Ultra-High Efficiency Topologies

This section presents several selected designs of various converter topologies targeting 48V to 12V conversion applications. The selected designs represent some of the best performance designs currently found in literature. Examining the commonalities and differences between these approaches allows for the key features enabling the design of ultra-high efficiency and high power density bus converters to be identified.

A. Conventional Buck Converter

As a point of comparison, a 48V to 12V Buck converter design is presented first. This design utilizes multiple phases, along with GaN FET devices, and represents a highly optimized Buck converter design with the highest power density demonstrated for a Buck converter in 48V to 12V conversion applications [30]. Fig. 5 shows a photo of one-phase of the Buck converter. It shows that inductor takes roughly 60% of the board area.

This reference design uses a 5-phase Buck converter to achieve 12V/60A (720W) output from 48V input. As shown in Fig. 6, this design achieves a full-load efficiency of around 95.8% (at 60A for five phases, or 12A for each phase), a peak efficiency of 96.2% (at 40A load current, or 7A each phase) and a power density of 1000W/in^3.

Despite using GaN FETs to switch at higher speeds and minimize the inductor size, the inductor will still take up more than 50% of the overall solution area. Of note for comparison later, this design uses 3.3µH inductors. This design operates at a nominal switching frequency of 500kHz and because of this high switching frequency and high voltage stress of the individual components, the light and medium load efficiency is relatively low, dominated by high switching losses despite using GaN FETs. It is also noted from Fig. 6 that at 5A load current (1A each phase current, or roughly 10% of the full load current), the efficiency is 88%, much lower than the peak efficiency and full load efficiency.

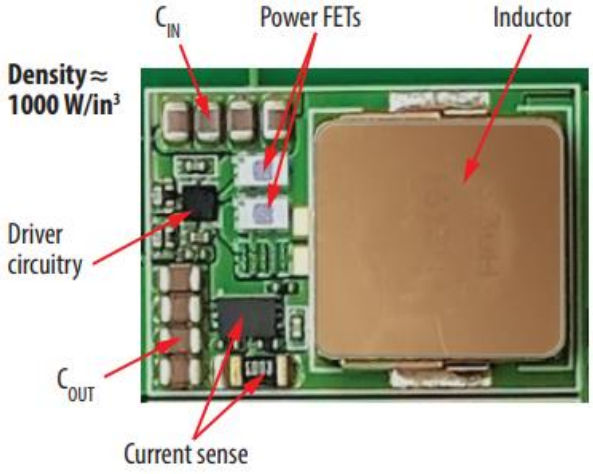

Fig. 5. EPC9130 Buck Converter - One-Phase, 1000W/in^3 prototype [30]

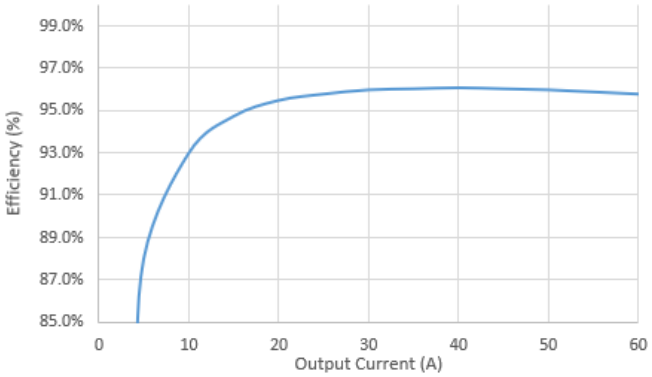

Fig. 6. EPC9130 Buck Converter - Efficiency [30]

B. LLC Resonant Converter

The LLC resonant converter is a well-known topology that offers significant benefits over a traditional buck converter design in many applications. Two LLC converter designs are presented here. The first demonstrates high power density of more than 1500W/in^3 but does not achieve efficiency of above 99%. The second design achieves efficiency of more than 99% but pays a huge penalty in terms of power density. These two highly optimized designs highlight the challenges of designing an ultra-efficient resonant converter, and clearly show that while good performance can be achieved, there is still room to improve to achieve both 99% efficiency and high power density of more than 1000W/in^3.

Fig. 7 shows the photo of the first LLC design presented in [31] by EPC. It offers clear benefits for 48V to 12V conversion as a

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bus converter when compared with the buck converter design above. The LLC design presented achieves a power density of 1500W/in^3, a peak efficiency of 98.3% for 48V/12V conversion, and full load efficiency of 97.8%, as shown in Fig. 8. In order to achieve such a high power density while using an LLC resonant converter topology, the switching frequency was selected at around 1MHz. This very high switching frequency makes it nearly impossible to achieve more than 99% efficiency, even when using GaN switching devices and a resonant topology that reduces the switching losses.

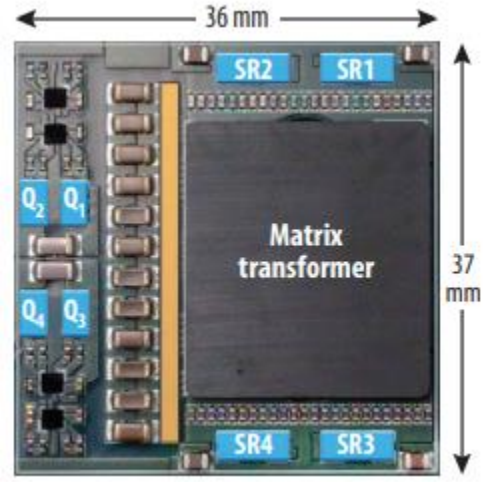

Fig. 7. EPC 900W LLC 1500W/in^3 Prototype [31]

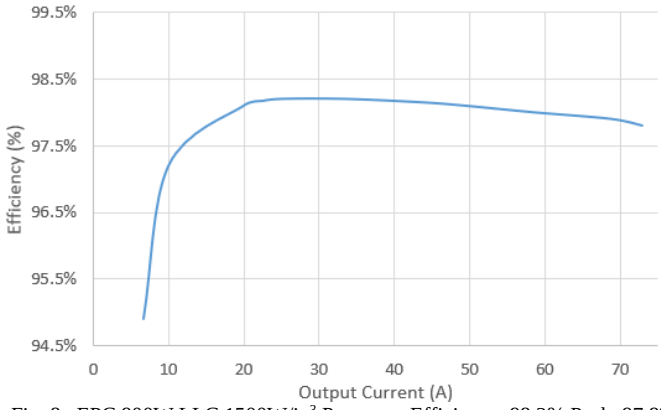

Fig. 8. EPC 900W LLC 1500W/in^3 Prototype Efficiency, 98.2% Peak, 97.8% Full Load 48V to 12V [31]

Even with resonant operation, in order to achieve ultra-high efficiency of more than 99%, the switching frequency must be reduced. This is demonstrated by the LLC DC-X design in [32], which represents an extremely high-performance resonant converter solution. The design presented is for 48V to 12V conversion for up to 3kW output and operates with a switching frequency of 500kHz. Fig. 9 shows the topology of the LLC DC-X converter.

The authors have spent a great deal of effort and multiple generations of refining and iterating this design (especially the transformer design), which illustrates both the potential of the LLC DC-X as well as how challenging it can be to achieve more than 99% efficiency with such a topology. As shown in Fig. 10, this design is able to achieve a peak efficiency of 99.1%, however, the power density is low at 450W/in^3.

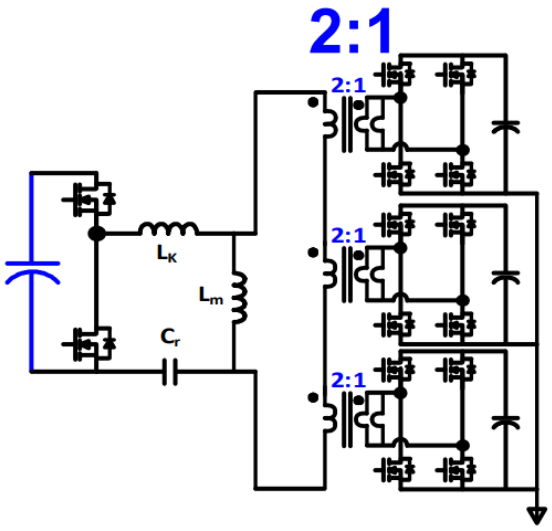

Fig. 9. LLC DCX Converter [32]

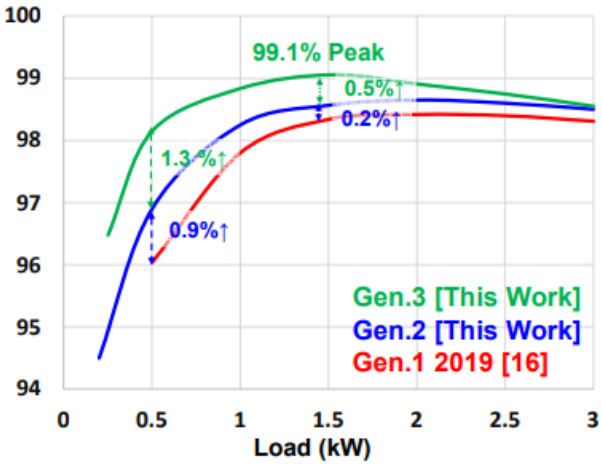

Fig. 10. LLC DCX Converter Efficiency, 99.1% Peak, 98.5% Full Load, 48V to 12V [32]

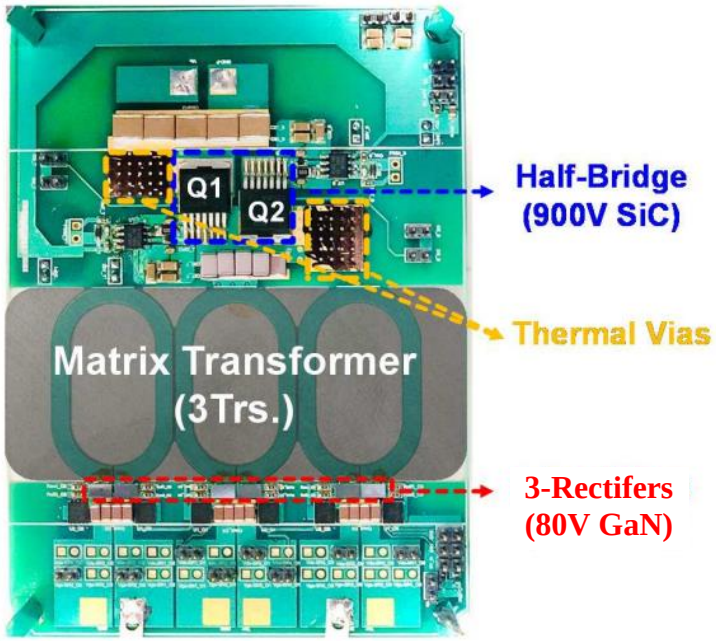

Fig. 11. LLC DCX Converter Prototype 450W/in^3

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The improvement in efficiency comes with a huge penalty in terms of size, due to the LLC converter's reliance on magnetic components, requiring both a transformer as well as resonant inductive elements.

Thus, while it is possible to achieve high efficiency with resonant converter designs, it is clear that even in highly optimized designs the overall reliance on magnetic components results in huge design trade-offs between size and efficiency. It is noted that this design uses 900V SiC MOSFET on the primary side to reduce the conduction losses of these devices (which is overkill), as well as GaN devices as synchronous rectifiers to reduce the secondary side conduction losses.

C. Switched Capacitor Converter

As mentioned in Section 1, many ultra-high efficiency topologies operate as non-isolated unregulated converters in bus converter applications. While there are many possible approaches, one of the more commonly investigated approaches recently are topologies based on the Switched-Capacitor Converter. The Switched-Capacitor Converter eliminates the magnetic components used in conventional topologies such as the Buck converter and instead uses capacitors to store energy and achieve voltage step-down or step-up. This is particularly desirable as even in the optimized Buck converter reference designs utilizing multiple phases, the inductor still dominates the overall size of the design.

Additionally, Switched Capacitor converter topologies typically utilize flying capacitors and switches arranged in a multi-level structure. By doing this, the voltage stress of individual switches is reduced. While the overall number of switches will be higher than in, for example, a Buck converter, the overall switching and conduction loss for the converter may be much lower in a Switched-Capacitor topology.

Unfortunately, the conventional Switched Capacitor topologies have a fundamental issue, known as charge redistribution [33]. As shown in Fig. 12, this charge redistribution occurs when the flying capacitors of the circuit are paralleled, and manifests as a large current spike caused by the slight voltage difference in the capacitors and the low impedance of the switch between them.

Mitigating the charge redistribution loss can be done through increased capacitor size, or by increasing switching frequency. However, as discussed in the previous section, operating at high switching frequencies is very difficult when ultra-high efficiency is desired.

Fig. 13 shows the design for a 4:1 Dickson Switched Capacitor Converter for 48V to 12V, 500W conversion with switching frequency of 200kHz, [35]. This design does achieve relatively high efficiency of 98% peak and nearly 97% full load (as shown in Fig. 14). Fig. 15 shows a photo of the prototype. It is noted that due to the low switching frequency, the flying capacitors are extremely large in order to mitigate the charge redistribution loss, and the power density achieved by this prototype is low ($400W/in^3$) when compared with other topologies that will be discussed and even with the conventional Buck converter design.

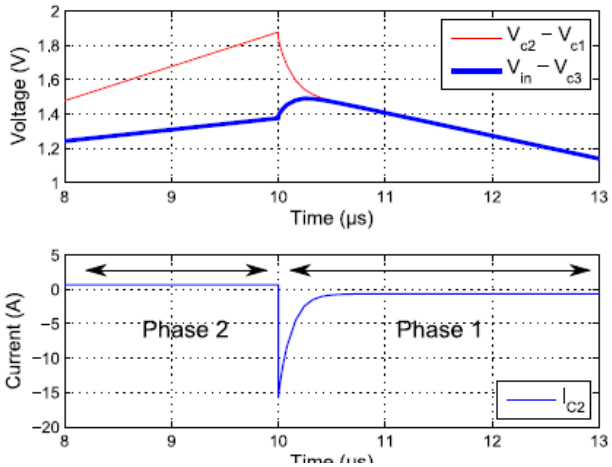

Fig. 12. Charge Redistribution in the Dickson Switched Capacitor Converter Referenced From [34]

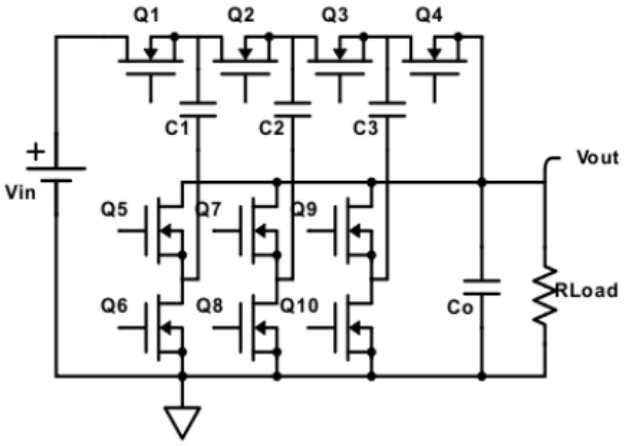

Fig. 13. 4:1 Dickson Switched Capacitor Converter [35]

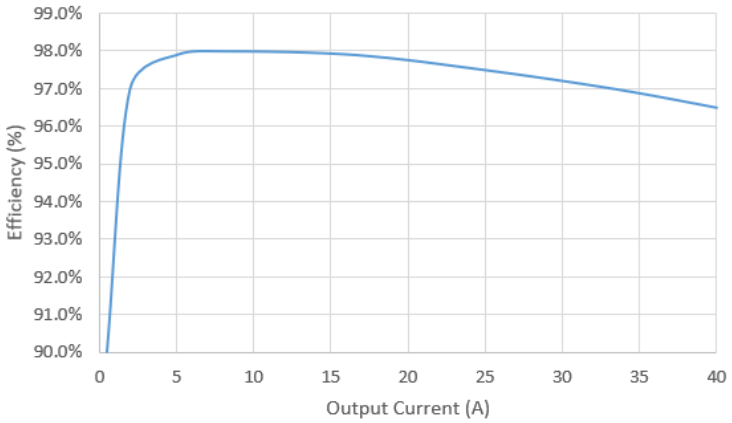

Fig. 14. 4:1 Dickson Switched Capacitor Converter Efficiency, 98% Peak, 97% Full Load [35], 48V to 12V

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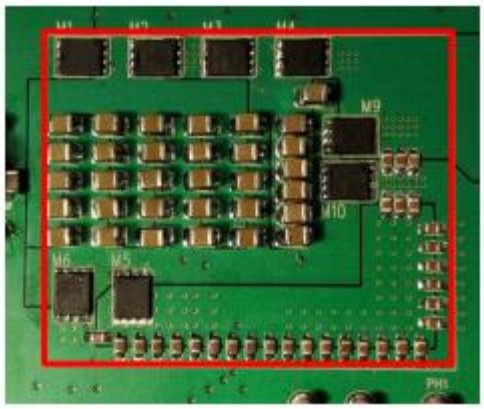

Fig. 15. 4:1 Dickson Switched Capacitor Converter Prototype, 400W/in^3 [35]

Traditional switched capacitor converter topologies, such as the Dickson Switched Capacitor Converter, therefore suffer from a similar design trade-off issue as topologies such as the buck converter, and LLC converter. The switching frequency of the Dickson converter must be increased in order to reduce the physical size of the converter and minimize the charge redistribution loss. However, the additional losses associated with this higher switching frequency mean that efficiencies above 99% cannot be achieved.

D. Cascaded Resonant Converter

In order to avoid the issues with charge redistribution loss, Switched Capacitor Converters with added inductive elements (often called Hybrid or Resonant Switched Capacitor Converters) have been developed [36-66]. While these topologies do add in an inductor, as compared with a Buck converter, the size of these inductors are very small, and are used to prevent the charge redistribution and/or to introduce resonant operation and reduce the switching losses. There are many topologies that follow this philosophy, but the Cascaded Resonant Switched Capacitor Converter [1-2], as shown in Fig. 16, has demonstrated the highest power density (2500W/in^3) and efficiency for this kind of topology thus far in literature and thus is selected here as an example.

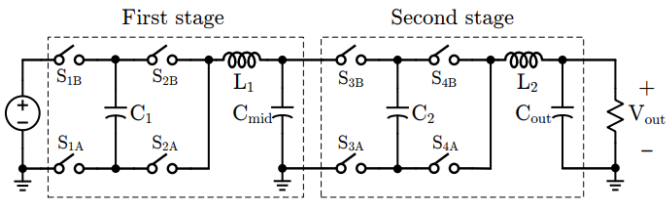

Fig. 16. Cascaded Resonant Switched Capacitor Converter [2]

This topology takes advantage of nearly all of the techniques mentioned in the previous section to achieve ultra-high efficiency and power density.

First, this topology benefits from the multilevel structure to reduce the voltage stress of the individual MOSFETs. The DC voltage of the flying capacitors C_1 and C_2 will reduce the voltage stress across each MOSFET to half of the input voltage (neglecting ripple). This significantly reduces the FOM for the switches.

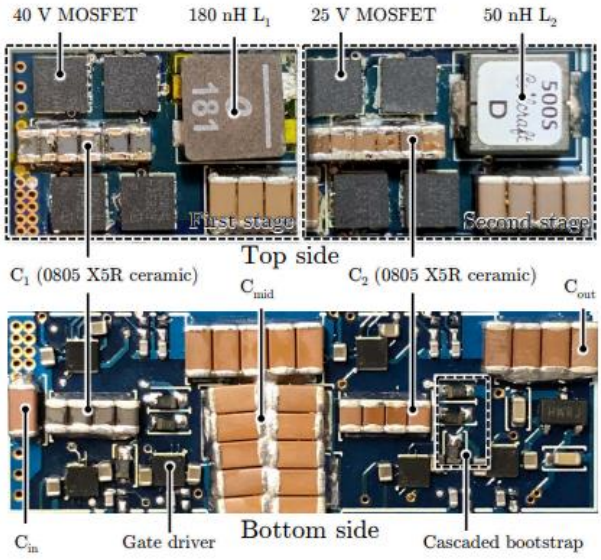

Fig. 17. Cascaded Resonant Converter, One-Phase 2500W/in^3 Prototype [1]

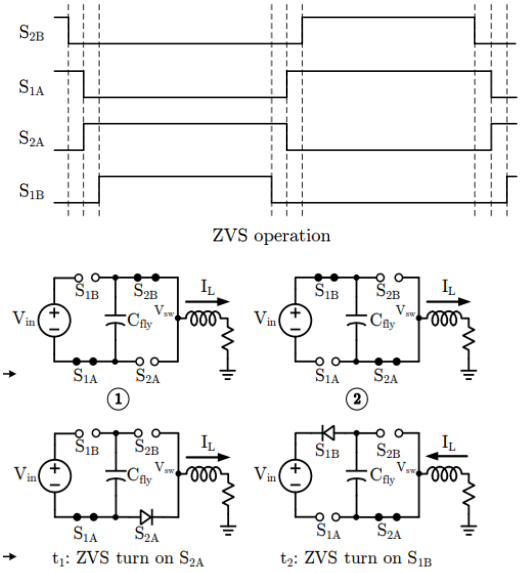

Fig. 18 Cascaded Resonant Switched Capacitor Converter Gate Drive Scheme and Switching States for ZVS Operation [2]

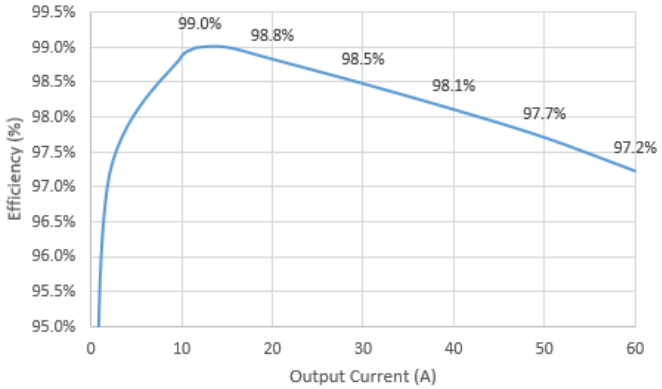

Fig. 19 Cascaded Resonant Switched Capacitor Converter Measured Efficiency, 99% peak, 97.2% Full Load 12V/60A

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Second, the resonant operation of the converter nearly eliminates the switching loss. Due to the unique topology, this resonant operation can be achieved using small inductors (L1 = 180nH and L2 = 50nH) operating at around 100kH.

Third, the converters can be easily paralleled to scale to different power levels. This is one of the very few tools a power designer has to reduce conduction losses, as splitting the current across two phases will halve the overall conduction loss. This converter also operates with full duty ratio (50% duty cycle on all switches, neglecting deadtime).

Fig. 17 shows a photo of the prototype. Fig. 18 gives the gate drive scheme and equivalent circuits at different stages. Fig. 19 shows the measured efficiency. Peak efficiency of 99% and full load (12V / 60A) efficiency of 97.2% have been achieved. The cascaded resonant converter therefore represents a clear example of a topology that follows the design philosophy summarized at the end of Section II.

Unlike the topologies discussed up to this point, the cascaded resonant converter is not faced with huge design trade-offs in terms of converter size and efficiency. The low volt-second seen by the inductors is an inherent feature of the topology, and without the charge redistribution loss the converter can be operated at low frequencies of approximately 100kHz. This low frequency operation allows for ultra-high peak efficiency of 99% to be achieved, while using capacitors as the primary energy storage devices in place of inductors allows for excellent power density.

E. Zero Inductor-Voltage Converter

While switched capacitor based topologies are one of the most commonly investigated topologies, there are other promising options to achieve ultra-high efficiency and power density. The Zero Inductor-Voltage (ZIV) converter [67], as shown in Fig. 20-25, operates in a fundamentally different way from the switched capacitor converter, despite having a similar structure at first glance. Fig. 21 shows the gate drive signals for all the switches, and Fig. 24 and 25 show the switching states of the ZIV converter.

As shown in Fig. 24 and 25 the flying capacitors in this circuit are never placed in parallel, meaning additional inductive elements are not required to prevent charge redistribution loss. Similar to the Cascaded Resonant converter the flying capacitors reduce the MOSFET voltage stress to 1/2Vin and 1/4Vin. As shown in Fig. 4 this reduction in MOSFET stress allows for much higher performance switches to be used. Unlike the Cascaded Resonant converter, however, the additional inductor (L1) and capacitor (C_{mid}) are not needed to decouple the stages. The single output inductor of the ZIV converter sees only the ripple voltage of flying capacitors, meaning that the size of this inductor is very small and the ZIV converter achieves "full duty ratio". This topology also demonstrates some of the highest efficiency, even higher than the Cascaded Resonant converter (97.8% at 12V/60A vs 97.23%) and power density (2500W/in^3) yet achieved for 48V to 12V conversion.

In addition, unlike the Cascaded Resonant converter, the ZIV converter does not use resonant operation, which can simplify the design, and highlights the value of reducing the switching frequency to improve overall efficiency. The ZIV converter operates at lower switching frequency (60kHz) and despite not being a resonant converter achieves higher peak efficiency due to this reduced frequency. To minimize the conduction losses, the ZIV converter can also be easily paralleled, and all the switches operate at "full duty ratio". The inductor value used in prototype is only 200nH.

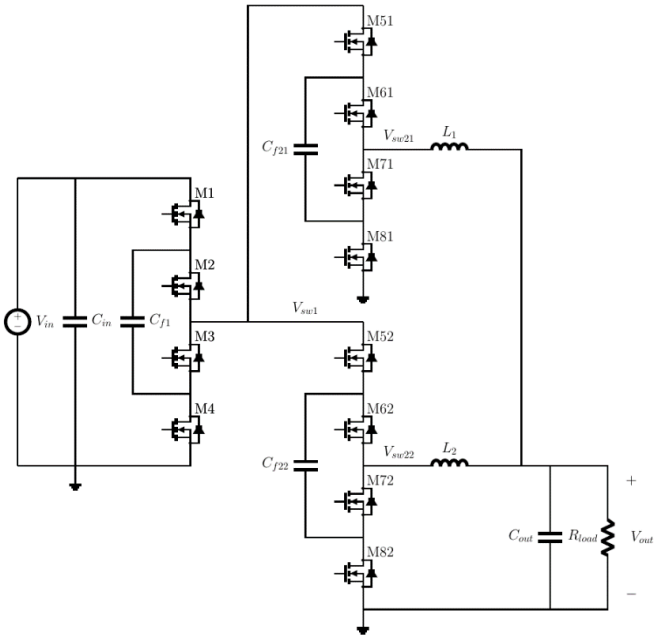

Fig. 20. Zero Inductor-Voltage Converter [67]

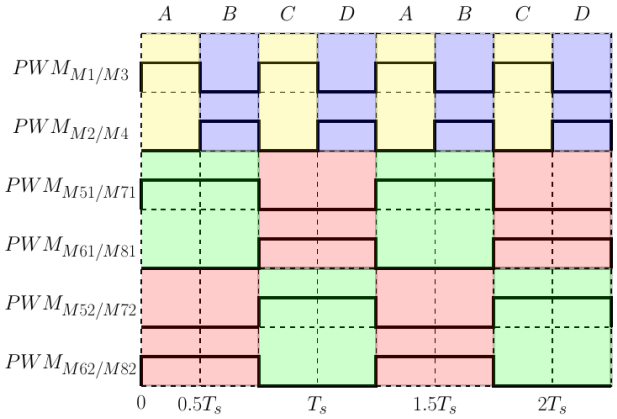

Fig. 21. Zero Inductor-Voltage Converter Gate Drive Scheme [67]

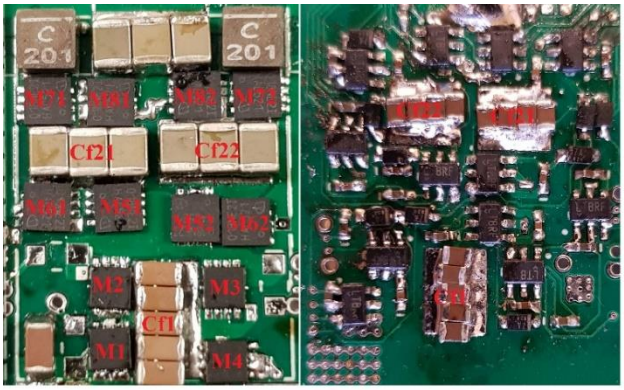

Fig. 22. ZIV Converter, One-Phase 2500W/in^3 Prototype [67]

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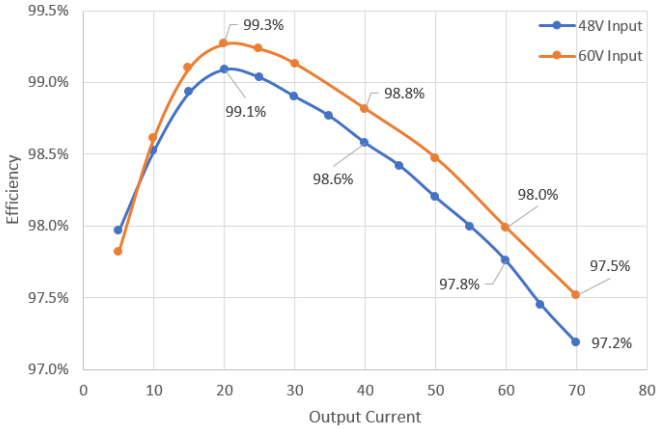

Fig. 23. Zero Inductor-Voltage Converter Efficiency, 99.1% Peak, 97.2% Full Load 12V/70A [67]

Much like the cascaded resonant converter the ZIV converter does not face a drastic design trade-off between converter size and efficiency. The output inductors see only the flying capacitor ripple voltage, so even below 100kHz the inductor size is orders of magnitude less than in a topology such as a buck converter. The power density demonstrated by this prototype is more than double that of a buck converter design, and more than 5 times better than an LLC converter design that also achieves 99% peak efficiency largely due to the reduction in magnetic components. In addition, the light load efficiency is also very high. At 5A load (7% of the full load), the efficiency is 98%.

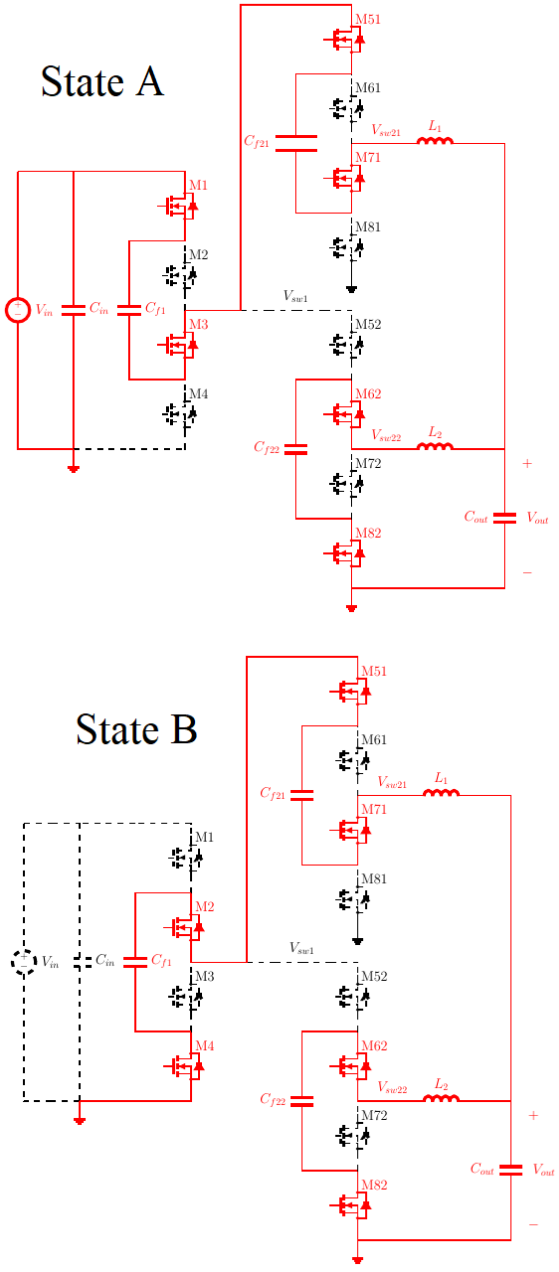

Fig. 24. Zero Inductor-Voltage Converter Switching States A and B

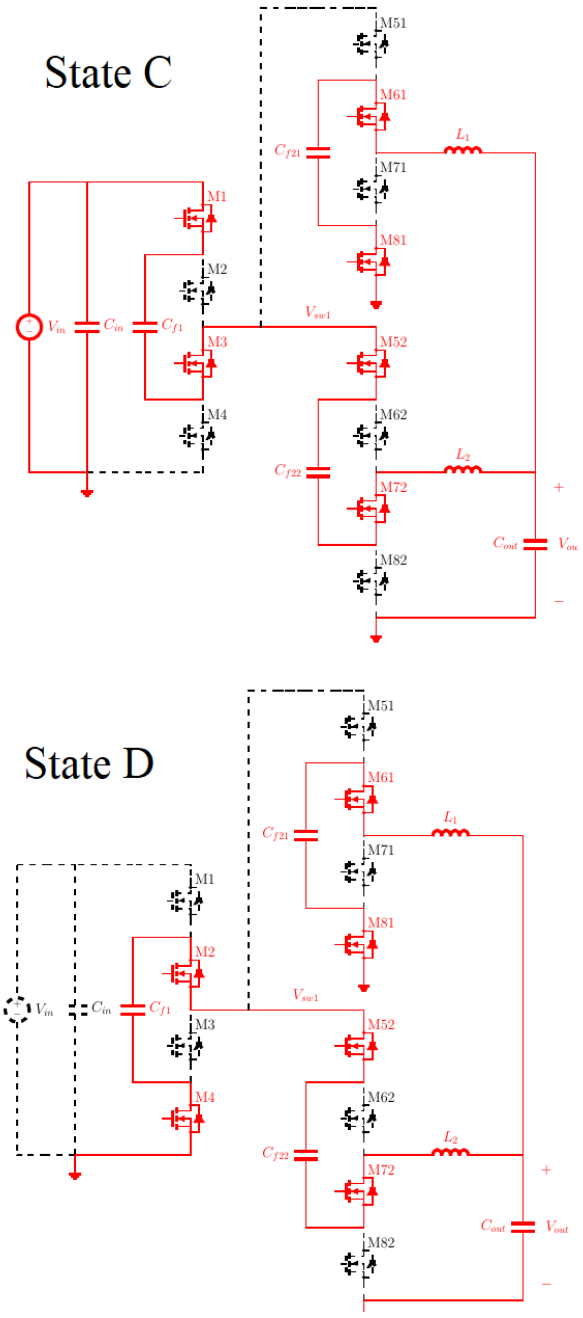

Fig. 25. Zero Inductor-Voltage Converter Switching States C and D

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IV. Conclusions

Achieving 99% efficiency and power densities on the order of 2kW/in^3 for DC-DC converters has gone from impossible, when considering conventional topologies, to demonstrated in laboratory conditions by several different prototypes in recent years. Many new topologies have been developed and continue to be developed to enable these incredible efficiency and power densities to be obtained. In particular, 48V to 12V conversion has been targeted as an application for next generation data centers, and research on this topic has led to extremely high performance experimental prototypes.

Resonant converter technologies such as the LLC converter have demonstrated the ability to achieve more than 99% efficiency with highly optimized magnetics designs and utilizing wide bandgap semiconductor devices, something that is not possible with a conventional buck converter. However, in achieving this high efficiency the power density of the resonant converter necessarily becomes very low, more than 5x less than the state-of-the-art. The LLC converter cannot be easily paralleled to reduce the conduction losses of the converter, and the switching devices see high voltage stress. The converters' large magnetic components, that make up approximately 50% of the volume of the board, prevent competitive power densities from being achieved.

Of the existing topologies that have demonstrated performance levels of more than 99% efficiency and 2kW/in^3 power density they share several key commonalities that highlight the key features we can currently understand as the enablers for ultra-high efficiency and power density. Tables 3 and 4 below highlight the concept that it can be desirable to increase the number of switches in a converter in order to reduce the reliance on magnetic components.

Table 3. Comparison of key characteristics from selected designs for several 48V to 12V converter topologies

	Buck	ZIV	Dickson	Cascaded Resonant	LLC DCX
Maximum Output Power (W)	720W	840W	480W	720W	3000W
Switching Frequency	500kHz	60kHz (120kHz)	200kHz	100kHz	500kHz
Regulated Topology	Yes	No	No	No	No
Resonant Operation	No	No	No	Yes	Yes

It is also clear that while resonant operation does provide advantages, it is more important to minimize the magnetic components in a topology and operate with low switching frequency (even if resonant operation is achieved). This is most clearly illustrated by the ZIV converter that achieves ultra-high efficiency without resonant operation. As discussed in Section I, operating as an unregulated topology is also critical for achieving ultra-high efficiency.

Table 4. Summary of key performance metrics from selected designs for several 48V to 12V converter topologies

	Buck	ZIV	Dickson	Cascaded Resonant	LLC DCX
Power Density (W/in^3)	1000	2500	400	2500	450
Peak Efficiency	96.0	99.1	98.0	99.0	99.1
Full Load Efficiency	95.8	97.2	96.8	97.2	98.5
# of Switches	10	**24**	10	**16**	14
Magnetics Volume	60%	5%	0%	10%	50%

. The ZIV converter and Cascaded Resonant converter take advantage of all of the following key enablers, without introducing new drawbacks such as charge redistribution in a conventional Switched-Capacitor converter, or utilizing bulky magnetics that reduce the power density:

- Easily Paralleled Design
- Multi-Level Structure
- Low Switching Frequency
- Full Duty Ratio
- Near Elimination of Magnetics (100x reduction)

These topologies, and other topologies that implement these features inherently avoid the huge design trade-offs that face many conventional converter designs wherein the converter efficiency must be sacrificed to achieve higher power density. As a result, these topologies offer ultra-high efficiency with power densities 5-6x higher than designs based on conventional topologies.

V. Acknowledgment

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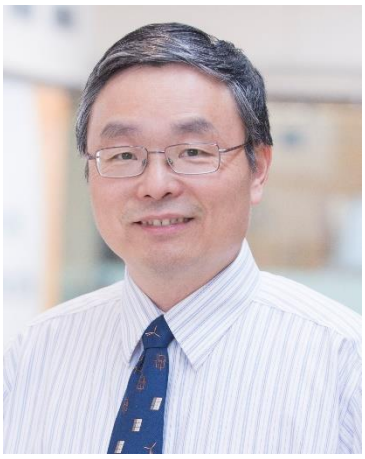
VII. BIOGRAPHIES



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