A Topology-Reconfigurable Fault-Tolerant Two-and-Single Stage AC–DC Converter for High Reliability Applications

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***Abstract*—A novel topology-reconfigurable two-and- single stage ac–dc converter with fault-tolerant capability for high reliability applications is proposed in this article. In the proposed converter, two bidirectional switches are used to connect the midpoints of the bridge branches between the rectifier stage and the dc–dc stage, and the proposed converter can be configured from the two-stage structure into the single-stage structure by turning on the bidirectional switches for the postfault conditions, therefore, the reliability of the power supply is reinforced. The two-stage structure for the normal condition works with an interleaved bridgeless power factor correction (PFC) rectifier and resonant dc–dc converter. The single-stage structure working under the postfault condition is made up of a PFC half-stage and resonant dc–dc half-stage, and the single-stage structure still has the same working performance as the two-stage structure. Operational principles, control scheme, and characteristics analysis of the topology-reconfigurable converter are analyzed. Finally, experimental results for both normal condition and postfault condition based on 1 kW prototype are provided to verify the effectiveness of the proposed converter.**

***Index Terms*—Interleaved power factor correction (PFC) rectifier, single-stage structure, topology-reconfigurable fault-tolerant ac–dc converter, two-stage structure.**

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I. Introduction

AC–DC converters are widely used in various applications, such as battery charger [1], [2], telecommunication power supply [3], LED driver [4], [5], renewable energy system [6], [7], and the more electric aircraft [8], [9]. In some applications, such as the telecommunication power supply, the more electric aircraft, the continuity of power supply is of vital importance. For that reason, a highly reliable power supply is required. The highly reliable power converters often depend on the fault-tolerant solutions to increase the reliability of the power converters, and the fault-tolerant solutions are usually based on the hardware redundancy with corresponding control strategy [10], [11].

The switching mode power converters are made up of magnetic elements, capacitors, and power semiconductor devices. Field experiences have demonstrated that the power semiconductor devices in switching mode power converters, such as insulated gate bipolar transistors and metal-oxide field-effect transistors (MOSFETs), are the most vulnerable components, which are potential threats to the reliability of the power converters [12], [13]. The failures of the power semiconductor devices are classified as the open circuit failure (OC) and the short circuit failure (SC) [14], which are caused by different reasons. The OC failures may be caused by the lifting of the bonding wires, a driver failure, or a short-circuit fault-induced rupture [14]. The SC failures may be caused by overvoltage, static or dynamic latch up, or energy shock. Since most of the conventional power converters do not have redundant design, any fault that occurred on the power devices can result in interruption of the system. Therefore, the power converters with fault-tolerant capability and enhanced system reliability attract research interest for the applications where the continuity of power supply is valued.

In order to increase the continuity of the power supply, quite a few of fault-tolerant converters are introduced for high reliability applications [15]–[22]. In [16], a comprehensive review of fault-tolerant topologies regarding power electronic converters in case of power device failures is presented. Four types of fault-tolerant solution in terms of hardware redundancy unit are reviewed and classified as: switch level, leg level, module level, and system level. The traditional fault-tolerant solutions are always based on the redundancy of hardware with corresponding control strategies [17], [18]. The redundancy of hardware with

corresponding control strategies will increase the system cost and the control complexity.

A fault-tolerant dc–dc converter based on reconfigurable resonant converter for solid-state transformer application is introduced in [19]. The introduced topology is based on configuring the full-bridge structure into half-bridge structure, and the output voltage is kept to its original value through configuring the full-bridge rectifier to voltage-double rectifier. Nevertheless, the failure type of the switches is required to be SC failure, and the other switch ON the same bridge should keep open. The presented topology is not suitable for the OC failure. Costa et al. [20] presented a family of fault-tolerant dc–dc converter derived from the resonant converter. The failure type of the switches is also required to be the SC failure. A fault-tolerant dc–dc converter based on three-level boost converter is introduced for photovoltaic (PV) application in [21]. The fault-tolerant strategy requires a bidirectional switch and the three-level boost converter will turn into two-level boost converter when failure occurs. The solution is efficient and the reliability is consequently reinforced. However, the voltage stress of the power switches is increased under the postfault condition. Soon et al. [22] introduced a nonisolated dc–dc topology to reinforce the reliability of dc–dc converter. The proposed solution is based on a buck converter and a redundant switching bridge is added to realize the fault-tolerant capability.

In order to increase the reliability of ac–dc converters, a novel topology-reconfigurable converter is proposed in this article. The major contribution of this article is to propose a topology-reconfigurable fault-tolerant ac–dc converter, which can increase the reliability of power supply. One contribution is that the proposed converter can be configured from the two-stage structure into the quasi-two-stage or the single-stage structure automatically by controlling the directional switch for the postfault condition, in consequence the reliability is reinforced. Furthermore, the normal condition and the postfault condition share the same control strategy. A steady-state analysis for pulsewidth modulation (PWM) controlled *LLC* resonant converter is presented to analyze the single-stage structure, which is used to analyze the voltage stress of the power switches under the postfault condition. Finally, experimental results and efficiency curves based on 1 kW laboratory prototype are given to demonstrate the feasibility of the proposed topology.

The rest of this article is organized as follows. In Section II, the proposed topology-reconfigurable fault-tolerant converter, operation principles of the two-stage and single-stage structure are analyzed in detail. In Section III, the characteristics of the single-stage structure is analyzed. The experimental results with efficiency curves are given in Section IV, which demonstrate the feasibility of the proposed topology. Finally, Section V concludes this article.

II. Proposed Topology-Reconfigurable Fault-Tolerant Converter and Operation Principles

A. Proposed Topology-Reconfigurable Fault-Tolerant AC–DC Converter and Circuit Description

The proposed topology-reconfigurable fault-tolerant ac–dc converter is shown in Fig. 1, the proposed topology consists

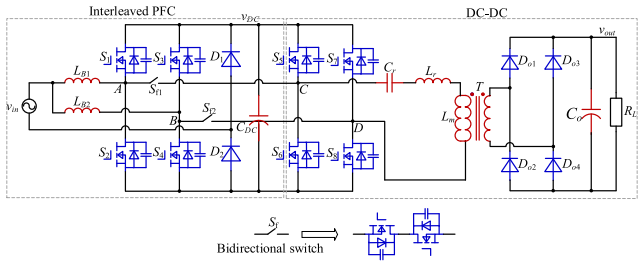

Fig. 1. Proposed topology-reconfigurable fault-tolerant converter.

of an interleaved bridgeless power factor correction (PFC) rectifier, an *LLC* resonant converter and two bidirectional switches. The bidirectional switches, which are made up of anti-series MOSFETs, are used to connect to the midpoints of the bridge branch between the front-end PFC rectifier and the *LLC* resonant dc–dc converter. The proposed topology works in the two-stage structure under the normal condition and will turn into the quasi-two-stage or the single-stage structure automatically by controlling the directional switch under the postfault condition. As shown in Fig. 1, L_{B1}, L_{B2} are the input filter inductors, $C_{\rm dc}$ is the dc-link capacitor, L_r is the resonant inductor, C_r is the resonant capacitor, and T is the high frequency transformer with magnetizing inductance L_m. The bidirectional switches S_{f1} and S_{f2} will be switched OFF under the normal condition; whenever there is fault occurred on the switches, the directional switches S_{f1} and S_{f2} will be switched on and the proposed converter will change into quasi-two-stage or single-stage structure for the postfault condition.

B. Control Strategy

The control strategy of the proposed topology-reconfigurable converter is shown in Fig. 2. The switching frequency of the proposed converter is the same as the resonant frequency. The duty cycle D allocated to the power switches S_1–S_4 is calculated in (1) to realize PFC according to the input voltage [23], [24]. As shown in Fig. 2(a), the converter works with an inner current loop and an outer voltage loop to correct the shape of the input current and regulate the output voltage, while leave the intermediate dc-link voltage unregulated. PWM signal is assigned to the power switches by comparing the modulation wave with an interleaved triangular wave. The duty cycle allocation scheme for the power switches S_1–S_4 is shown in Fig. 2(b): 1-D is allocated to the switches S_1 and S_3, and D is allocated to the switches S_2 and S_4 during the positive half-cycle; while D is allocated to the switches S_1 and S_3, and 1-D is allocated to the switches S_2 and S_4 during the negative half-cycle. The power switches S_5–S_8 of the resonant dc–dc converter work in complementary mode at the resonant frequency

$$D = 1 - \left| \frac{v_{\rm in}}{v_{\rm dc}} \right| \tag{1}$$

where $v_{\rm in}$ is the ac input and $v_{\rm dc}$ is the output.

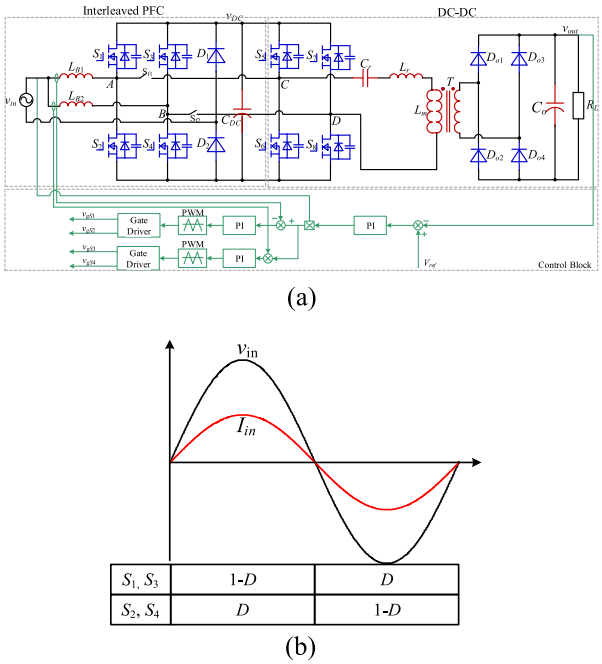

Fig. 2. Control strategy. (a) Control scheme. (b) Duty cycle D allocation scheme.

C. Family of the Topology-Reconfigurable Fault-Tolerant AC–DC Converter

A family of the topology-reconfigurable fault-tolerant AC–DC converter is shown in Figs. 3 and 4. If an OC fault occurred on any of the power switches, and the midpoints of the branch are connected by closing the bidirectional switch, the system can continue to operate.

1) Quasi-Two-Stage Structure With One Faulty Switch: In Fig. 3, an assumption is made that there is one faulty switch occurred in the converter and the normal two-stage structure is turned into the quasi-two-stage structure by closing S_{f1} or S_{f2} in this scenario.

2) Single-Stage Structure With Two Faulty Switches: In Fig. 4, an assumption is made that there are two faulty switches occurred in the converter and the normal two-stage structure is turned into a single-stage structure by closing S_{f1} and S_{f2} at the same time in this scenario. It can be noticed that the quasi-two-stage structure can also be turned into the single-stage structure by closing the bidirectional switches S_{f1} and S_{f2} at the same time. In addition, the quasi-two-stage structure can change into the single-stage structure in the event of a second failure.

D. Operation Principles for the Postfault Condition

The operation principles of the single-stage structure for the postfault condition are analyzed in this part. The control scheme expressed in Fig. 2 is still effective and can be used for both of quasi-two-stage and the single-stage structure.

The operation principles of the single-stage structure illustrated in Fig. 4(d) are analyzed in this part. In Fig. 4(d), switches S_3, S_4, S_5, S_6 are kept open due to the faults occurred on the power switches, and switches S_1, S_2, S_7, S_8 keep working

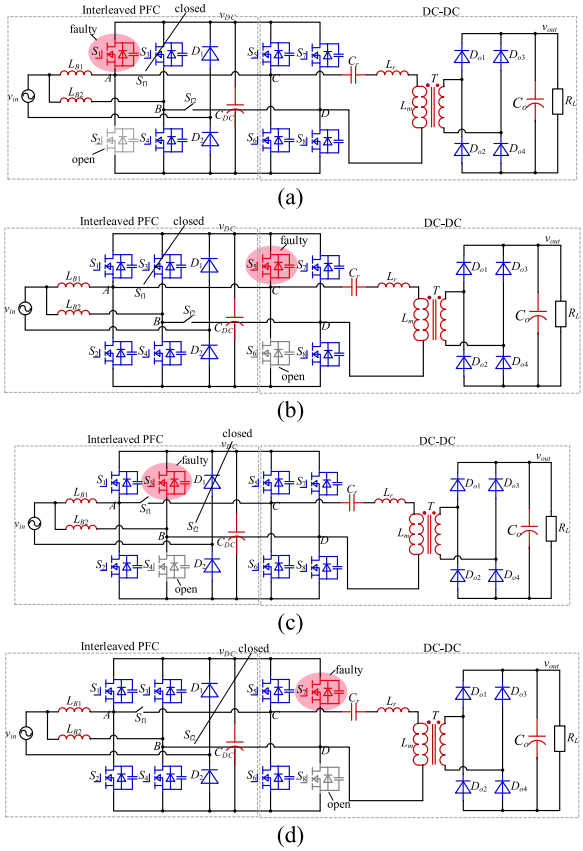

Fig. 3. Family of the quasi-two-stage structure with one faulty switch. (a) Fault occurred on the first bridge branch. (b) Fault occurred on the third bridge branch. (c) Fault occurred on the secondary bridge branch. (c) Fault occurred on the fourth bridge branch.

as an interleaved single-stage ac–dc converter. The operational modes of the proposed single-stage are presented as follows.

Fig. 5 shows the operational modes of the single-stage structure, the resonant tank will be directly connected to the PFC stage by turning ON the bidirectional switches. The single-stage structure consists of the rectifier half-stage and the resonant dc–dc half-stage, the control strategy, and duty cycle allocation scheme expressed in Fig. 2 is still effective in the single-stage structure. For sake of simplicity, Fig. 5(a)–(d), which are the operation modes during the positive half-cycle of the input voltage are presented in this section, the diode D_2 conducts while diode D_1 is blocked during this half-cycle.

Fig. 6 shows the operational waveforms of the single-stage structure, the gate-driving signals for the power switches S_3, S_4, S_5, and S_6 are blocked. v_{gs1}, v_{gs2}, v_{gs7}, and v_{gs8} are the gate-driving signals for the power switches S_1, S_2, S_7, and S_8. The phase shift angle between switch S_1 and S_7 is 180°. i_{Lr} is the resonant current. i_D is the output rectified current. t_0-t_1 are the instants when the power switches commutate.

Stage 1 [$t_0 \le t < t_1$; see Fig. 6(a)]: When switch S_1 turns ON, this stage starts. In the PFC half-stage, the input inductor L_{B1} charges the dc-link capacitor with current i_{LB1} decreasing linearly, and the input voltage charges the input inductor L_{B2}

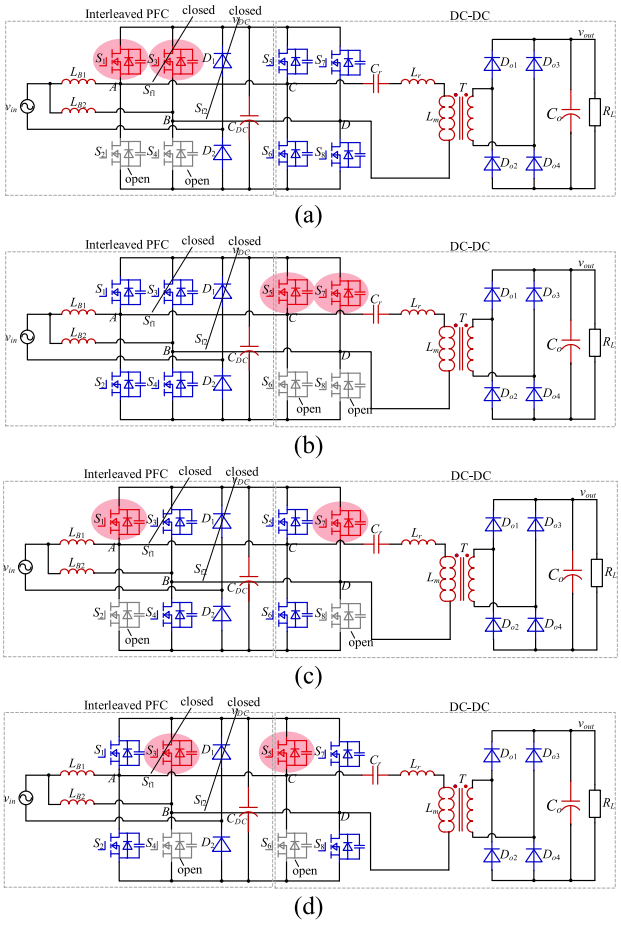

Fig. 4. Family of the single-stage structure with two faulty switches. (a) Faults occurred on the PFC branches. (b) Faults occurred on the *LLC* branches. (c) Faults occurred on the first and fourth bridge branches. (d) Faults occurred on the secondary and third bridge branches.

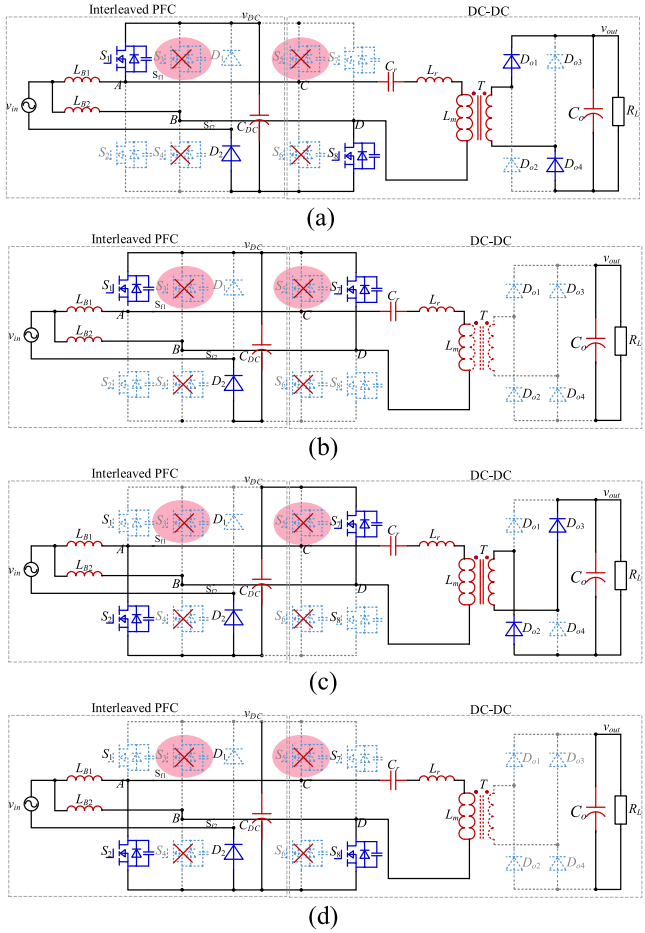

Fig. 5. Operational modes of the single-stage structure under the postfault condition. (a) Stage 1 ($t_0 \le t < t_1$). (b) Stage 2 ($t_1 \le t < t_2$, D<0.5). (c) Stage 3 ($t_2 \le t < t_3$). (d) Stage 4 ($t_1 \le t < t_2$, D>0.5).

with current i_{LB2} increasing linearly. In the *LLC* resonant half-stage, the voltage between A and B v_{AB} is $+v_{\rm dc}$, the resonant inductor L_r resonates with the resonant capacitor C_r. The diodes D_{o1} and D_{o4} are conducting, and the primary voltage of the transformer T is clamped by $nv_{\rm out}$. The difference between the resonant current and the magnetizing current is transferred to the secondary side.

Stage 2 [$t_1 \le t < t_2$; see Fig. 6(b) or (d)]: When switch S_7 turns ON and S_8 turns OFF, this stage starts. In the PFC half-stage, the inductors L_{B1} and L_{B2} charges the dc-link capacitor at the same time with currents i_{LB1} and i_{LB2} decreasing linearly. v_{AB} is 0 and the resonant current is equal to the magnetizing current, and there is no energy transferred to the secondary side.

Stage 3 [$t_2 \le t < t_3$; see Fig. 6(c)]: When switch S_1 turns OFF and S_2 turns ON, this stage starts. Symmetric to Interval 1, the input voltage charges input inductor L_{B1} with current i_{LB1} increasing linearly. L_{B2} charges dc-link capacitor with current i_{LB2} decreasing linearly. Voltage v_{AB} is $-v_{\rm dc}$, the resonant current i_{Lr} varies in the sinusoidal waveform. The diodes D_{o2} and D_{o3} are conducting, the primary voltage of the transformer T is clamped at $-nv_{\rm out}$, and the magnetizing current i_{Lm} decreases linearly by the reflected voltage.

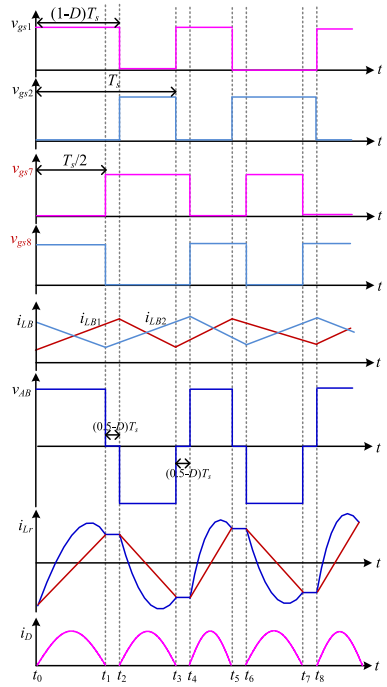

Fig. 6. Principal waveform of the fault-tolerant operation.

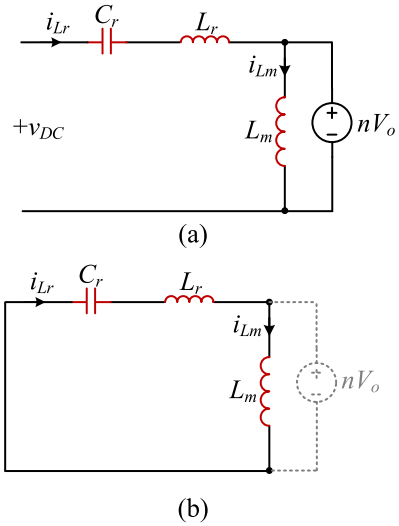

Fig. 7. Equivalent circuit of the *LLC* resonant tank. (a) Equivalent circuit of stage 1. (b) Equivalent circuit of stage 2.

III. Characteristics Analysis of the Proposed Topology

The characteristics of the proposed topology-reconfigurable fault-tolerant topology are analyzed in this section. In the front-end PFC stage, the interleaving operation can double the ripple frequency of the input current and reduce the input current ripple, as analyzed in [23] and [24]. In the single-stage structure, PWM is applied to the *LLC* resonant half-stage, and conventional FHA [25], [26] is no longer appropriate for the PWM-controlled *LLC* resonant converter. This section presents an analysis method based on the steady-state analysis of the PWM-controlled *LLC* resonant half-stage to calculate the voltage stress of the power switches for the postfault condition.

First, the differential equations based on the equivalent circuit during the switching period are set up; second, the solutions to the differential equations are obtained based on solving the equations. And the voltage gain of the PWM-controlled *LLC* resonant tank is obtained, and it can be used to calculate the voltage stress of the dc-link capacitor and the power switches.

The equivalent circuit during one switching period is presented in Fig. 8. During stage 1, the transformer is clamped by the output voltage nv_{out}, and the difference between the resonant current and the magnetizing current is transferred to the secondary side. During stage 2, the input voltage of the resonant half-stage is 0, and there is no energy transferred to the secondary side.

The differential equations for stage 1, as shown in Fig. 7(a), are expressed as follows:

$$\begin{cases} v_{Cr}(t) + L_r \frac{di_{Lr}(t)}{dt} = v_{\text{dc}} - nv_{\text{out}} \\ C_r \frac{dv_{Cr}(t)}{dt} = i_{Lr}(t) \\ L_m \frac{di_{Lm}(t)}{dt} = nv_{\text{out}} \\ i_p(t) = i_{Lr}(t) - i_{Lm}(t) \end{cases}. \tag{2}$$

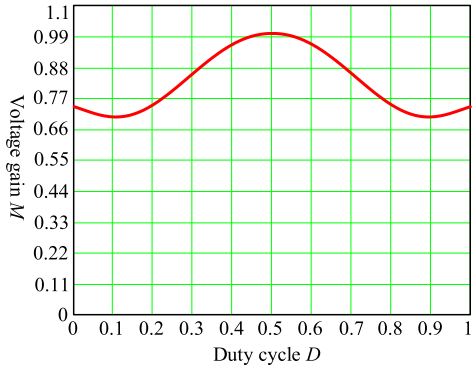

Fig. 8. Voltage gain M of the PWM-controlled *LLC* resonant tank *vs* duty cycle D with full load.

The solutions to (2) are obtained

$$\begin{cases} v_{Ct}(t) = [v_{Cr}(t_0) - (v_{\text{dc}} - nv_{\text{out}})]\cos\omega_r(t-t_0) \\ \qquad +Z_o i_{Lr}(t_0)\sin\omega_r(t-t_0) + v_{\text{dc}} - nv_{\text{out}} \\ i_{Lr}(t) = \frac{(v_{\text{dc}} - nv_{\text{out}}) - v_{Cr}(t_0)}{Z_o}\sin\omega_t(t-t_0) \\ \qquad +i_{Lr}(t_0)\cos\omega_r(t-t_0) \\ i_{Lm}(t) = i_{Lm}(t_0) + \frac{nv_{\text{out}}}{L_m}(t-t_0) \end{cases}. \tag{3}$$

In (3), Z_o is defined as the characteristic impedance of the *LLC* resonant tank, and ω_r is the resonant angular frequency, which are defined as follows:

$$\begin{cases} Z_o = \sqrt{\frac{L_r}{C_r}} \\ \omega_r = \frac{1}{\sqrt{L_r C_r}} \end{cases}. \tag{4}$$

The differential equations for stage 2, as shown in Fig. 14(b), are expressed as follows:

$$\begin{cases} v_{Cr}(t) + (L_r + L_m)\frac{di_{Lr}(t)}{dt} = 0 \\ i_{Lr}(t) = C_r \frac{dv_{Cr}(t)}{dt} \\ i_{Lr}(t) = i_{Lm}(t) \\ i_p(t) = 0 \end{cases}. \tag{5}$$

The solutions to (5) are obtained as

$$\begin{cases} v_{Cr}(t) = v_{Cr}(t_1)\cos\omega_m(t-t_1) \\ \qquad +i_{Lr}(t_1)\sqrt{\frac{L_r+L_m}{C_r}}\sin\omega_m(t-t_1) \\ i_{Lr}(t) = -v_{Cr}(t_1)\sqrt{\frac{C_r}{L_r+L_m}}\sin\omega_m(t-t_1) \\ \qquad +i_{Lr}(t_1)\cos\omega_m(t-t_1) \\ i_{Lm}(t) = i_{Lr}(t) \end{cases}. \tag{6}$$

In (6), ω_m is defined as the resonant angular frequency of L_r, L_m, and C_r

$$\omega_m = \frac{1}{\sqrt{(L_r + L_m)C_r}}. \tag{7}$$

The symmetry and continuity of the resonant current is expressed as follows:

$$\begin{cases} i_{Lr}(0) = i_{Lm}(0) \\ i_{Lr}(t_1) = i_{Lm}(t_1) \end{cases} \tag{8}$$

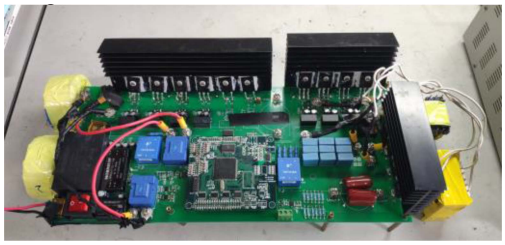

Fig. 9. Experimental prototype of the two-stage converter.

$$\begin{cases} i_{Lr}(t_1) = -i_{Lr}(0) \\ v_{Cr}(0) = -v_{Cr}(t_2) \end{cases}. \tag{9}$$

Ignore the power loss during the power transmission, the input average power and the output power are calculated as follows:

$$P = \frac{\int_0^{T_s/2} v_{AB} \cdot i_{Lr}(t)dt}{T_s/2} = \frac{v_{\text{out}}^2}{R_L}. \tag{10}$$

By solving the abovementioned equations, the voltage gain of the PWM-controlled resonant half-stage is obtained as (11) shown at the bottom of this page, where the R_L is load, K_A, K_B, K_A are the coefficients defined as follows (12) shown at the bottom of this page.

In (12), Δt and t_1 is expressed by the switching frequency f_s and duty cycle D as follows:

$$t_1 = \begin{cases} \frac{D}{f_s} & 0 < D \le 0.5 \\ \frac{1-D}{f_s} & 0.5 < D < 1 \end{cases} \tag{13}$$

$$\Delta t = t - t_1 = \left|\frac{1}{2} - D\right| \cdot \frac{1}{f_s}. \tag{14}$$

The duty cycle D in (13) and (14) is calculated in (1) to realize PFC.

Fig. 8 shows the relationship between the voltage gain M of the resonant half-stage and the duty cycle D under the full load condition. And the voltage stress of the dc-link capacitor and the power switches can be calculated based on the voltage gain.

IV. Experimental Results and Verification

A. Experimental Prototype

An 1 kW SiC MOSFET-based laboratory prototype is fabricated and tested to verify the feasibility of the proposed topology-reconfigurable converter. Fig. 9 shows the experimental prototype of the proposed converter. The bridgeless totem-pole PFC rectifier and an *LLC* resonant converter are fabricated in the experimental prototype. The control scheme is implemented in DSP (TMS320F28335) from Texas Instruments. And the main components used in the experimental prototype are listed in Table I. The input voltage of the prototype is $v_{\text{in}} =$ 110 Vac–220 Vac 50/60 Hz and the dc output voltage is $v_{\text{out}} =$ 400 Vdc.

TABLE I
Key Components Used in the Experimental Test-Bed

Components	Values
Input voltage (v_{in})	110VAC-220VAC 50/60Hz
Output voltage (v_{out})	400V
Rated output power	1kW
Input inductor (L_{B1}=L_{B2})	1mH
Resonant inductor (L_r)	37μH
Resonant capacitor (C_r)	68nF
Turn ratio (n)	1:1
Magnetizing inductance (L_m)	120μH
Resonant frequency (f_r)	100kHz
Switching frequency (f_s)	100kHz
Intermediate capacitor	390μF
Output capacitor (C_{out})	1500μF

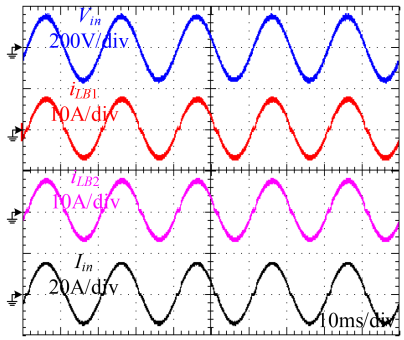

Fig. 10. Input voltage V_{in}, inductor current i_{LB1}, i_{LB2}, and input current I_{in} at 110 Vac input with full load.

B. Experimental Results for the Normal Condition

Figs. 10–12 present the experimental waveforms of the two-stage structure for the normal condition. Fig. 10 shows the input voltage V_{in} along with the inductor current i_{LB1}, i_{LB2} and the input current I_{in} at 110 Vac input with full load.

$$M = \frac{v_{\text{out}}}{v_{\text{DC}}} = \frac{K_B R_L + K_C R_L - nK_A R_L + \sqrt{(K_B R_L + K_C R_L - nK_A R_L)^2 + 4K_A R_L}}{2} \tag{11}$$

$$\begin{cases} K_A = \frac{[1+\cos(\omega_m \Delta t)][1-\cos(\omega_r t_1)]}{\pi Z_o [1+\cos(\omega_r t_1)\cos(\omega_m \Delta t)]} \\ K_B = \frac{-nt_1\left[Z_o \sin(\omega_r t_1)\cos(\omega_m \Delta t) - \sqrt{\frac{L_r+L_m}{C_r}}\sin(\omega_m \Delta t)\right][1-\cos(\omega_r t_1)]}{2\pi Z_o L_m [1+\cos(\omega_r t_1)\cos(\omega_m \Delta t)]} \\ K_C = \frac{-nt_1 \sin(\omega_r t_1)}{2\pi L_m} \end{cases} \tag{12}$$

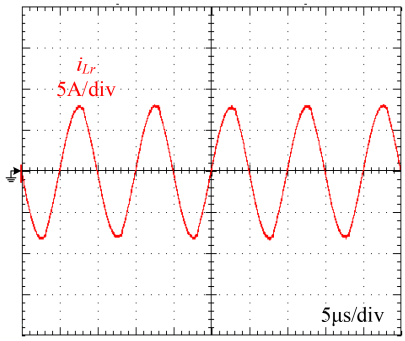

Fig. 11. Resonant current i_{Lr} with full load.

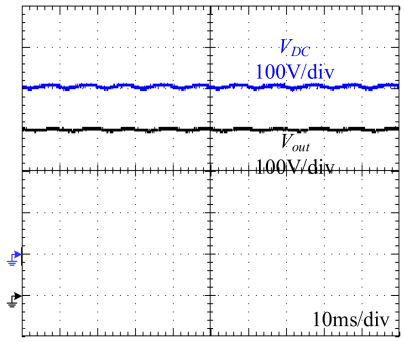

Fig. 12. Intermediate dc-link voltage $v_{\rm dc}$ and 400 Vdc output with full load.

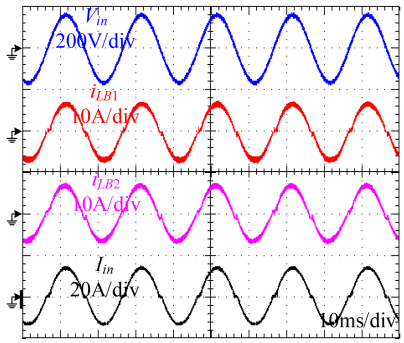

Fig. 13. Input voltage $V_{\rm in}$, inductor current i_{LB1}, i_{LB2}, and input current I_{in} under 110 Vac input with full load.

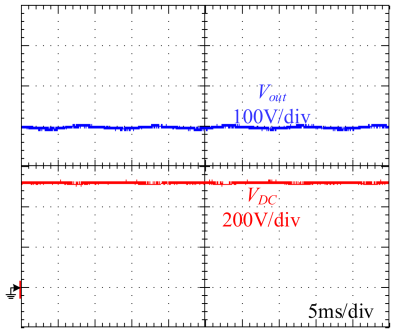

Fig. 14. Intermediate dc-link voltage $v_{\rm dc}$ and 400 Vdc output with full load.

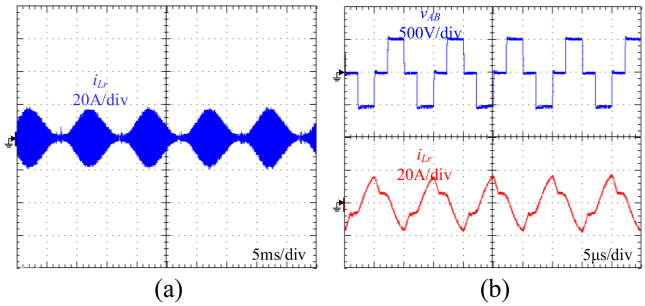

Fig. 15. Resonant current i_{Lr}. (a) Time scale: 5 ms/div. (b) Time scale: 5 μs/div.

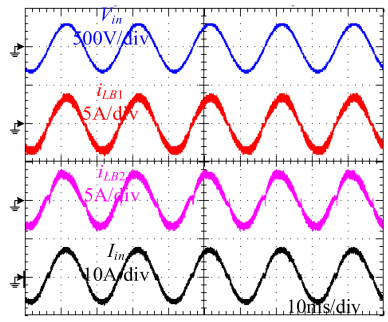

Fig. 16. Input voltage $V_{\rm in}$, inductor current i_{LB1}, i_{LB2}, and input current $I_{\rm in}$ under 220 Vac input with full load.

Fig. 11 shows the resonant current i_{Lr} of the resonant tank, the resonant current i_{Lr} varies in a sinusoidal shape by the resonance of the resonant inductor and the resonant capacitor. Fig. 12 shows the dc-link voltage $v_{\rm DC}$ and the dc output $v_{\rm out}$, which are both at 400 Vdc.

C. Experimental Results for the Postfault Condition

1) Experimental Waveforms at 110 Vac Input: Figs. 13–15 show the experimental waveforms of the single-stage structure for the postfault condition with 110 V input voltage. Fig. 13 shows the input voltage $V_{\rm in}$ along with the inductor current i_{LB1}, i_{LB2} and the input current I_{in} under 110 Vac input with full load. Fig. 14 shows the measured dc-link voltage $v_{\rm dc}$ and the output voltage $v_{\rm out}$, and it is demonstrated that the output voltage $v_{\rm out}$ is still regulated as 400 Vdc.

Fig. 15 shows the resonant current i_{Lr} in different time scales. Fig. 15(a) demonstrates that the envelope of the resonant current is the sinusoidal shape with the time scale 5 ms/div, and Fig. 15(b) demonstrates that the high-frequency pulsating voltage of the *LLC* resonant tank and the resonant current in detail with time scale 5 μs/div, which proves that the resonant current are still high-frequency components.

2) Experimental Waveforms at 220 Vac Input: Figs. 16–18 show the experimental waveforms of the single-stage structure for the postfault condition with 220 Vac input. Fig. 16 shows the input voltage $V_{\rm in}$ along with the inductor current i_{LB1}, i_{LB2} and the input current I_{in} at 220 Vac input with full load. Fig. 17 shows the measured dc-link voltage $v_{\rm dc}$ and the dc output $v_{\rm out}$,

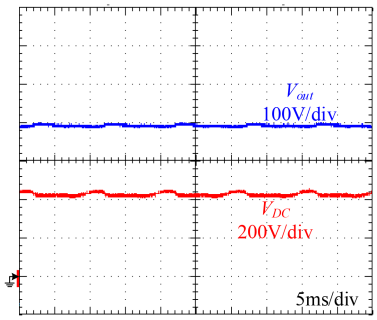

Fig. 17. Intermediate dc-link voltage $v_{\rm dc}$ and 400 Vdc output with full load.

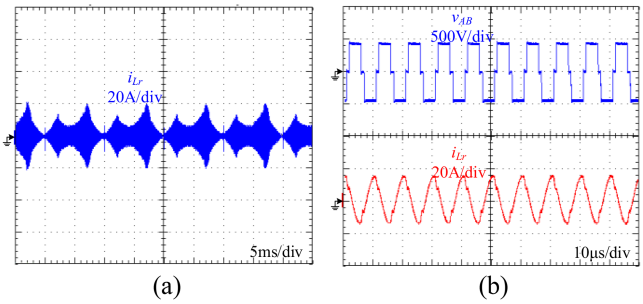

Fig. 18 Resonant current i_{Lr}. (a) Time scale: 5 ms/div. (b) Time Scale: 10 μs/div.

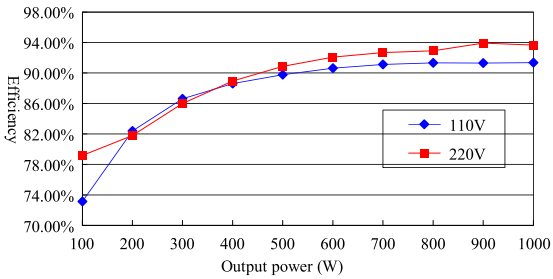

Fig. 19. Efficiency of the normal condition with two stage.

which demonstrates that the output voltage $v_{\rm out}$ is still controlled as 400 Vdc.

Fig. 18 shows the resonant current i_{Lr} in different time scales. Fig. 18(a) demonstrates that the envelope of the resonant current is the sinusoidal shape with the time scale 5 ms/div, Fig. 18(b) demonstrates that the high-frequency pulsating voltage of the *LLC* resonant tank and the resonant current in detail with time scale 10 μs/div, which proves that the resonant current are still high-frequency components.

D. Efficiency

Efficiency curves of both the two-stage structure and the single-stage structure at 110 Vac and 220 Vac input are presented in Figs. 19 and 20, respectively. Fig. 19 shows the efficiency curve of the two-stage structure for the normal condition, and Fig. 20 shows the efficiency curve of the fault-tolerant single-stage structure for the postfault condition.

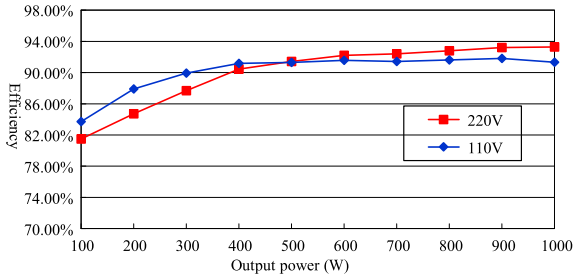

Fig. 20. Efficiency of the postfault condition with single-stage structure.

V. Conclusion

A fault-tolerant converter was proposed to increase the reliability of the power supply. The proposed topology-reconfigurable two-and-single stage converter operates in the two-stage structure for the normal condition and will be configured into the single-stage structure by controlling the bidirectional switches for the postfault condition. The normal two-stage structure and the postfault single-stage structure share the same control strategy, therefore, the control complexity was not increased. Finally, experimental results based on an 1 kW experimental prototype with 110—220 Vac input and 400 Vdc output are presented to verify the feasibility of the proposed converter. The proposed converter can realize fault-tolerant operation, which can increase the reliability of the power supply. However, the proposed converter has limitations. The proposed converter works only for the open-circuit failure and it requires more components, which impacts the cost and volume.

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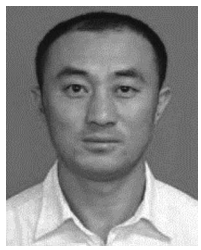

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