A Line Cycle Synchronous Rectification Strategy Based on Time-Domain Analysis for Single-Stage AC–DC LLC Converters

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***Abstract*—Synchronous rectification that is being widely used in high power and current DC-DC *LLC* resonant converters to reduce conduction losses can be challenging in single-stage AC-DC *LLC* converters with high output voltage levels (i.e., >200 V) where synchronous rectifier (SR) driving ICs cannot be used. In this paper, a simple AC line cycle synchronous rectification strategy with direct control by a cost-effective microcontroller unit (MCU) is proposed for single-stage AC-DC *LLC* converters with high switching frequencies using wide bandgap devices (i.e., GaN or SiC). The SR gate pulse is generated based on the time-domain calculated conduction time, which is then switched ON and OFF over the AC line cycle to avoid reverse power flow in light load conditions. The proposed strategy reduces the complexity of implementation over any adaptive online calculation or model-based methods that require powerful and expensive MCUs. First, the operation is briefly described followed by the time-domain analysis for AC operation. Next, the calculation and methodology behind the proposed AC line cycle SR driving strategy are discussed in detail. A scaled-down wide bandgap-based AC-DC *LLC* converter prototype with a 250–400 V output voltage range is used with digital control implementation to validate the performance of the proposed synchronous rectification strategy. It is found that maximum efficiency of 98.1% can be achieved which is improved by around 0.5% over the conventional fixed conduction time method. Moreover, it is shown that the proposed method obtains the same efficiency levels as more complex adaptive SR driving approaches.**

***Index Terms*—Efficiency improvement, gallium nitride (GaN) high electron mobility transistors (HEMT), LLC resonant converter, SiC MOSFET, Single-stage ac-dc, synchronous rectification, wide bandgap devices.**

I. Introduction

RESONANT converters have been the focus of many research studies over the past decades. A lot of researchers have devised various computer-aided methods based on frequency-domain analysis or time-domain analysis to optimize the resonant tank design for different applications [1], [2], [3], [4]. Some research studies focused on magnetics design modification and improvement for resonant converters and using integrated planar magnetics to improve power density [5], [6], [7]. Some researchers worked on the extension of input and/or output voltage operation for different applications by using hybrid switching strategies, using modified resonant tanks, and topology reconfiguration [8], [9], [10].

The recent trend in research shows significant interest in the impact of wide bandgap semiconductors, such as gallium nitride (GaN) high electron mobility transistors (HEMTs) and silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) in improving the efficiency and power density of resonant converters [11], [12], [13], [14]. GaN HEMTs have a small gate charge (Q_g) and output capacitance (C_{oss}) compared with typical Si MOSFETs, which allows a more desirable operation at high switching frequencies (i.e., hundreds of kHz). GaN HEMTs demonstrate various benefits in high-frequency soft-switching resonant converters from several aspects. In general, a large enough dead time is required for switches to achieve ZVS in resonant converters. Increasing the dead time reduces the effective turn ON time of the switch in a half-switching cycle and hence increases the rms current through the switch and magnetic windings, which will increase power losses [13] and [14].

Moreover, by increasing the switching frequency the dead time needs to be reduced and hence a higher magnetizing current is required to achieve ZVS, which demands a smaller magnetizing inductance. This will generally increase circulating current and power loss in resonant converters. By using GaN switches a small dead time can be used with larger magnetizing inductance and smaller air gap and less fringing loss in the windings, which is because GaN switches can turn ON and OFF much faster than Si switches. Moreover, GaN devices depending on their type have little to no reverse recovery charge which makes them a suitable choice for resonant converters in light load conditions. As in *LLC* resonant converters, the turn OFF current of the primary switches does not reduce in light load conditions, to maintain the ZVS operation of Si devices it is required to expand the optimal full load deadtime so the body diode of MOSFETs has enough time to fully reset before the other switch can be turned ON [14].

Another key contributor to the efficiency performance of resonant converters is output rectification loss. In high power and high output current dc–dc resonant converters diode conduction loss is a major contributor to the total power conversion loss.

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Hence, using synchronous rectification is a necessity for low voltage and high current applications to achieve high conversion efficiency at kW levels. Therefore, a lot of research has been done on synchronous rectification for dc–dc *LLC* converters as it is necessary to implement an effective synchronous rectifier (SR) driving strategy for different applications [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30]. One of the common practices for SR driving in resonant converters is hardware-based drain-source voltage sensing using SR driving ICs, such as NCP4306 [15]. This method is widely used in many low-voltage high-current applications [16], [17], [18], [19]. The performance of driving ICs is promising in most cases; however, it can be highly dependent on the effect of parasitic components of the circuit that reduces the reliability of the converter and requires special attention in the converter design process [18]. On the other hand, the maximum available voltage rating for the sensing pin of these ICs is limited to 200 V and hence they are not suitable for SR driving at higher output voltage levels. In [19], some additional components are added to the well-known NCP4306 SR driving IC to make it work for above 200-V output voltage applications, however, the disadvantages of low voltage sensing still exist. In [20], an analytical adaptive SR driving strategy based on drain-source voltage sensing is proposed to solve inaccuracies in the turn OFF instant. In this method, the turn ON instant is recognized based on the body diode conduction, and to consider the layout stray inductance effect some conduction time compensation is calculated based on measuring the primary side resonant current to calculate an accurate turn OFF instant. This method relies on multiple sensing and measurements, such as low voltage sensing, resonant current sensing, and recording time which can introduce error and is not cost-effective.

Another hardware-based practice for SR driving is by sensing the primary side current to emulate the secondary side current to generate the SR driving signal, which is more immune to noise or circuit parasitic effects than voltage sensing methods [21], [22], [23]. In [21], an extra parallel inductor is added at the primary side of the transformer with a much smaller inductance than the magnetizing inductor so the primary side current of the transformer can be sensed with a current transformer to drive the SRs. In [22], the primary resonant current and the magnetizing current on the secondary side are sensed using an extra winding to generate the SR driving signals. Another similar current sensing method is introduced in [23] by using additional windings on the resonant inductor and the transformer and an integrator circuit to emulate the secondary current so proper SR gate signals can be generated for every operating point. Although these methods seem to be the most reliable methods for both below-resonant and above-resonant applications they are not cost-effective as additional current sensing circuits are needed that are also not so efficient for high-power applications.

Recognition of the power delivery stage in the *LLC* converter based on comparing the polarity of the inverter voltage and the transformer secondary voltage is called homopolarity SR modulation which is another hardware-based SR driving strategy [24]. In this method, the SR gate pulse is generated only when the polarity of the inverter bridge and the secondary side voltage is the same. There are two drawbacks related to this method, first is in the above resonant region early turn OFF happens, and second in below resonant operation in light load conditions early turn ON can happen as this method cannot distinguish between power delivery and freewheeling stage in light load. Another power delivery recognition method is based on resonant capacitor voltage sensing [25]. In this method, the integration of the capacitor voltage, input and output voltages are used to generate the SR driving pulses which have noise immunity and can be used for all operating modes. The only drawback of this method is that three voltage sensing is needed and complex control implementation.

Contrary to hardware-based approaches, researchers have extensively investigated software-based strategies using the microcontroller unit (MCU) to drive the SRs [26], [27], [28], [29], [30]. The software-based approach is mainly developed on prediction using model-based calculations that enable the generation of appropriate gate pulses based on the converter condition. In [26], the SR driving signal is generated based on the primary bridge signals using a simulation model to find out the turn ON and OFF delays that were inserted into a 3-D look-up table for all the operating conditions. In [27], a rather fixed conduction time is used with specific turn ON and OFF delays for the *LLC* converter of an EV battery charger. In this approach, the output voltage and current should be considered to correctly reflect the output power and tune proper driving signal delays accordingly to avoid inaccurate gate signals. In [28], an online calculation method is used to turn OFF the SRs based on the switching frequency and load. In the mathematical calculations, it is assumed that the operation is at resonant which leads to an inaccurate calculation for switching frequencies far away from the resonant frequency.

In [29], an adaptive sensor-less model-based digital driving scheme is developed for the dc–dc *LLC* converter. In this method, the output voltage and current are sensed to find out the load condition, then using the switching frequency, the conduction time of the SR is calculated cycle by cycle based on a frequency domain mathematical model for both above-resonant and below-resonant operations. In [30], an impedance calculation method is used to calculate the output impedance of the resonant tank at the load side so the SR conduction time can be calculated. Then the calculation is implemented in a powerful MCU to do a cycle-by-cycle SR conduction time calculation. One drawback of this method is that only the first harmonics are considered in the calculation which can lead to large deviations over wide operating voltage and load ranges. It should be mentioned that in the software-based approaches where look-up tables are utilized a low-cost MCU can handle the SR modulation, however, in all the online calculation methods more powerful and costly microprocessors are required.

So far, most of the literature regarding SR driving of *LLC* resonant converters only discussed the dc–dc operation. In recent years, there is a significant interest in the implementation of the *LLC* converter in either single-phase or three-phase single-stage ac–dc conversion with power factor correction (PFC) capability, which is mainly because ac–dc *LLC* converters can be designed to achieve minimum switching losses [31], [32], [33], [34],

[35], [36]. However, most of the literature either did not use synchronous rectification for low-power applications or used SR driving ICs for low-output voltage applications, such as low-voltage battery charging [35]. Only in [36], SiC MOSFETs are used in the output bridge of an electric vehicle on-board charger for charging the high voltage battery of the vehicle. Direct digital control from MCU is implemented in this work, with a fixed conduction time for the SRs over the line cycle. This method was not based on any calculation for conduction time and also incurs some reverse power flow at light load conditions over the ac line cycle, which increases conduction losses.

In the literature, the SR conduction behavior of the ac–dc *LLC* converters has never been investigated thoroughly over the ac line cycle. Near the ac voltage zero crossing (VZC) area, the input power delivered to the load is much smaller than the rated power, and in such light load conditions, both SR late turn ON and early turn OFF can happen which makes the SR driving of the *LLC* converter challenging. In such applications, hardware-based methods are less attractive due to their susceptibility to noise and false triggering for a light load operation, especially with high switching frequency implementation. Although for low output voltage conditions (e.g., <200 V) it is possible to use the same dedicated SR controller ICs as in dc–dc converters, this method is not transparent to the designer, is not immune to noise, and there is no full control over the driving signals. Based on the literature for dc–dc *LLC* converters in high output voltage applications either a hardware-based current sensing method that requires additional sensing circuits or a software-based cycle-by-cycle calculation method that requires a powerful MCU can be implemented for ac–dc *LLC* converter. Therefore, a proper simple low-cost SR driving strategy based on the ac performance is missing for ac–dc *LLC* converters to achieve enhanced power conversion efficiency for high-power applications with high output voltage levels and a high switching frequency range.

To address the abovementioned issues for the SR driving of ac–dc *LLC* converters a simple ac line cycle SR driving strategy is proposed in this article. The proposed method is a sensorless approach with digital driving signals generated directly from the MCU using accurate mathematical calculation results. It should be mentioned that ac line cycle time-domain analysis is used in this article to find out the SR conduction behavior of a wide output voltage range ac–dc *LLC* converter. The salient feature of the proposed ac line cycle driving strategy is its simplicity of implementation in low-cost MCUs that makes it suitable for high-frequency implementation and independent of the output voltage level. In Section II of this article, a brief description of the *LLC* converter operation for PFC applications is discussed first that is followed by a time-domain analysis of the *LLC* converter for ac–dc applications. The detailed analysis of the proposed synchronous rectification strategy for different output voltage and load levels is discussed in Section III. Experimental results of a digitally controlled wide bandgap-based scaled-down laboratory prototype are provided in Section IV to first verify and then compare the performance of the proposed ac line cycle SR driving strategy with a more complicated alternative solution. Finally, Section V concludes this article.

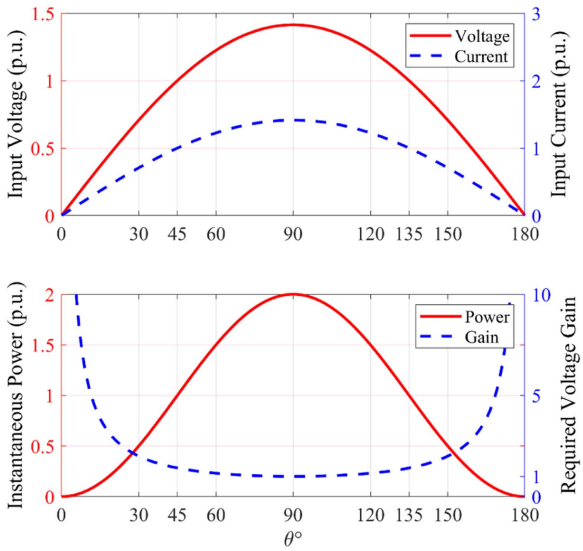

Fig. 1. Theoretical per unit representation of voltage, current, power, and the required voltage gain of a PFC converter over the ac line half cycle.

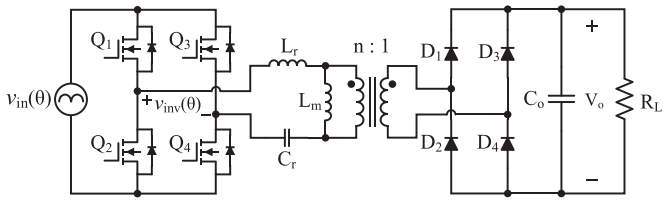

Fig. 2. Single-stage full-bridge LLC resonant converter with PFC operation.

II. Analysis of Single-Stage AC–DC LLC Converter

In this section, a brief overview of the operation of the *LLC* converter with PFC functionality is provided. Fig. 1 illustrates the per-unit voltage and current of a unity power factor rectifier with a pure sinusoidal shape over the ac line half cycle. The resulting per unit instantaneous power is shown in the bottom row of Fig. 1 and it can be observed that at the peak line voltage (i.e., $\theta = 90°$) the power requirement is double the average rectifier output power. Moreover, the required voltage gain to achieve power factor correction is shown with a dashed line in the bottom row of Fig. 1. It should be mentioned that around VZC the required voltage gain is high to achieve proper PFC and avoid distortion in the input current shape, and at ac line peak voltage the minimum voltage gain is required that is set to unity in this figure. Later it will be shown graphically by design gain curves how the *LLC* converter can meet the PFC voltage gain requirement.

A. Analysis of LLC Converter for Power Factor Correction Operation

Fig. 2 illustrates the full-bridge *LLC* resonant converter with a full-bridge output rectifier. The source voltage to the input inverter bridge is a time-varying voltage based on the rectified ac voltage with a double-line frequency ripple. In many applications, it is desired to operate the *LLC* converter in the inductive

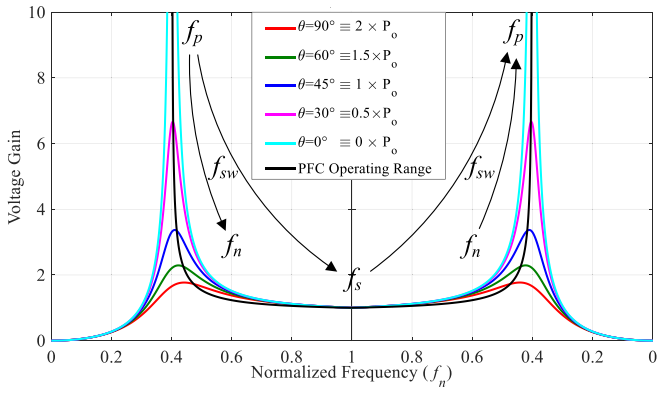

Fig. 3. Voltage gain characteristic of the LLC tank operating between the series resonant frequency and parallel resonant frequency to satisfy the voltage gain requirement for a PFC operation.

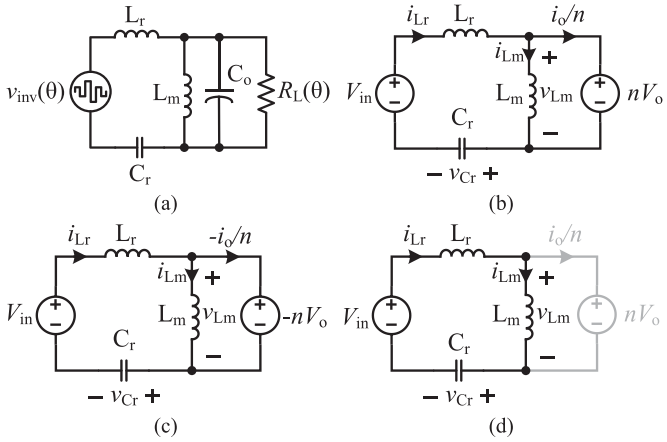

Fig. 4. Equivalent circuit of the LLC resonant tank over (a) the AC line operation, and the positive half switching cycle in (b) stage P, (c) stage N, and (c) stage O.

region with frequencies above the parallel resonant frequency (f_p) to make sure the inverter bridge switches can achieve zero voltage switching (ZVS). On the other hand, the voltage gain of the *LLC* tank has a slow slope above the series resonant frequency (f_s) and hence does not help in PFC operation, where large voltage gain variation is required. Moreover, above f_s the output rectifiers lose zero current switching (ZCS) which is not preferred. Hence, a proper desired operating range can be defined between the parallel resonant frequency and series resonant frequency to maintain soft-switching and high voltage gain variation. A detailed mathematical analysis for the PFC operation of the *LLC* resonant converter can be found in [26].

Fig. 3 illustrates the voltage gain curves of the *LLC* resonant converter for different output power levels corresponding to different ac line phase angles (θ) over the ac line half-cycle operation. The transformer turn ratio is designed based on the lowest required output voltage level and the peak line voltage as it is desired that the voltage gain of the *LLC* tank does not go below unity. When designing for a wide output voltage range, the highest required voltage gain by the *LLC* tank should be met by the peak line voltage operation at double output power in the design curves shown in Fig. 3. Over the ac line half cycle operation when regulating the lowest designed output voltage the switching frequency varies from f_p at $\theta = 0°$ to f_s at $\theta = 90°$ and then goes back to f_p at $\theta = 180°$. For the highest designed output voltage, the switching frequency varies from f_p at $\theta = 0°$ to a specific f_n at $\theta = 90°$ that is corresponding to the highest required *LLC* tank gain and then goes back to f_p at $\theta = 180°$.

B. Time-Domain Analysis of the LLC Converter for AC–DC Operation

Due to variable switching frequency and load conditions over the ac line cycle, the ac–dc *LLC* converter operates in various modes consisting of one or more operating stages. In order to analyze the ac line cycle operation, the line cycle can be discretized and each slice can be studied based on its own dc characteristics. Then, a discrete operating condition with its corresponding switching frequency can be solved for each line phase angle that can provide ac time-domain behavior when added together. Fig. 4(a) illustrates the equivalent circuit of the *LLC* tank over the ac line cycle where the inverter bridge voltage and the output load are dependent on the ac line phase angle θ. Moreover, as the output capacitor is acting as an energy storage component in ac–dc operation and contributing to the power transfer, it should be included in the time-domain analysis to consider output voltage fluctuation. However, as it is considered that the input and output voltages are constant in each slice of the ac line cycle, each operating stage of the *LLC* tank can be analyzed in dc conditions without an output capacitor considered.

The operational stages of the *LLC* resonant tank are symmetrical in the positive and negative half-switching cycles. Hence, to simplify the analysis, only the operational stages of the *LLC* tank during the positive half-switching cycle when Q_1 and Q_4 are turned ON are discussed. According to the states of the output rectifier diodes, three operational stages are known as the "P" stage which stands for positive when the diodes D_1 and D_4 are turned ON and a positive output voltage is applied to the magnetizing inductor; the "N" stage which stands for negative when the diodes D_2 and D_3 are turned ON and a negative output voltage is applied to the magnetizing inductor and the O stage which stands for OFF when all the diodes are turned OFF and the magnetizing voltage is not clamped to the output. The equivalent circuit of the *LLC* resonant tank in different operating stages is illustrated in Fig. 4(b) to (d).

From Fig. 4(b) it can be observed that in the P stage, the voltage across the magnetizing inductor is clamped by the positive output voltage nV_o and hence i_{Lm} increases linearly, L_r and C_r are in resonance ($f_r = 1/(2\pi\sqrt{L_r C_r})$). Using the Kirchhoff's voltage law (KVL) on the *LLC* equivalent circuit shown in Fig. 4(b), the P stage can be modeled with a second-order differential equation. From Fig. 4(b) the following state equations can be written:

$$\begin{cases} v_{Cr}(t) = V_{in} - L_r \frac{di_{Lr}(t)}{dt} - nV_o \\ i_{Lr}(t) = C_r \frac{dv_{Cr}(t)}{dt} \\ i_{Lm}(t) = \frac{1}{L_m} \int_0^t nV_o dt + i_{Lm}(t_0) \\ i_o(t) = n \times (i_{Lr}(t) - i_{Lm}(t)). \end{cases} \quad (1)$$

Then the resonant inductor and capacitor voltages can be derived by solving the second-order differential equations in the P stage, which is only valid for $t_0 < t < t_1$. Depending on the operation mode, when the first stage is the P stage $t_0 = 0$ and $t_1 = t_P \times T_{sw}/2$, where t_P is the ratio of the P stage duration over the half-switching cycle. At resonance, we have only P mode operation and t_1 in this mode is equal to the desired SR conduction time. However, when there is an O stage before the P stage $t_0 = t_O \times T_{sw}/2$ and $t_1 = (t_O + t_P) \times T_{sw}/2$, where t_O is the ratio of the O stage duration over the half-switching cycle.

In the O stage, the secondary side rectifier is disconnected from the primary side and there is no power delivery to the load. In this stage, L_m also joins the resonance with L_r and C_r. Moreover, i_{Lr} is equal to i_{Lm} and hence the resonant frequency becomes $f_{rm} = 1/(2\pi\sqrt{(L_r + L_m)C_r})$. From Fig. 4(d) the following state equations can be written:

$$\begin{cases} v_{Cr}(t) = V_{in} - L_r \frac{di_{Lr}(t)}{dt} - v_{Lm}(t) \\ i_{Lr}(t) = C_r \frac{dv_{Cr}(t)}{dt} \\ v_{Lm}(t) = L_m \frac{di_{Lm}(t)}{dt}. \end{cases} \tag{2}$$

Then, the resonant inductor current, magnetizing inductor current, and resonant capacitor voltage can be derived for the O stage, which is only valid for $t_1 < t < t_2$. Depending on the operation mode, the O stage can occur before a P stage or after that. Hence, $t_1 = 0$ and $t_2 = t_O \times T_{sw}/2$ for a preceding O stage and $t_1 = t_P \times T_{sw}/2$ and $t_2 = T_{sw}/2$ for a succeeding O stage. In this stage, $|v_{Lm}|$ should be smaller than nV_o to avoid turning on the rectifier diodes.

In some heavy load conditions with marginal ZVS design, it is likely to observe the N stage in the positive half-switching cycle. In this case, the voltage across the magnetizing inductor is clamped by -nV_o and hence i_{Lm} decreases linearly, and L_r and C_r are in resonance. Using KVL on the *LLC* equivalent circuit shown in Fig. 4(c), the N stage can be modeled with a second-order differential equation as follows:

$$\begin{cases} v_{Cr}(t) = V_{in} - L_r \frac{di_{Lr}(t)}{dt} + nV_o \\ i_{Lr}(t) = C_r \frac{dv_{Cr}(t)}{dt} \\ i_{Lm}(t) = \frac{-1}{L_m} \int_0^t nV_o dt + i_{Lm}(t_2) \\ i_o(t) = -n \times (i_{Lr}(t) - i_{Lm}(t)). \end{cases} \tag{3}$$

Then the resonant inductor and capacitor voltages for this stage can be derived by solving the second-order differential equations, which are only valid for $t_2 < t < t_3$. Depending on the operating mode when the N stage comes after a P stage $t_2 = t_P \times T_{sw}/2$ and $t_3 = T_{sw}/2$ (i.e., for PN mode), and when the N stage comes after an O stage $t_2 = (t_P + t_O) \times T_{sw}/2$ and $t_3 = T_{sw}/2$ (i.e., for PON mode).

Since t_O and t_P are not fixed and depend on the load and switching frequency, they cannot be considered constant to calculate the *LLC* voltage gain (M) and initial conditions of the resonant current and voltage values of the *LLC* converter. Therefore, the voltage gain, initial resonant current, and voltage values should be found dependent to t_O, t_P, and switching frequency (f_{sw}). As mentioned in the previous subsection, it is desired to operate the ac–dc *LLC* converter below the resonant to take advantage of ZCS. At the below resonant frequency, there are different operating modes as O, OPO, PO, PON, and PN. The PO mode is the main operating mode, while OPO mode and O modes can happen at light load and no-load conditions, respectively. The N stage which usually happens in a very short time can only happen at heavy loads around the *LLC* tank peak gain with a marginal ZVS design which is not desirable due to the possibility of losing ZVS. Therefore, to avoid PN and PON modes in the design procedure the peak power delivery for the highest output voltage condition should be checked in the design procedure. In other PFC operation conditions, the *LLC* tank peak gain is only required around the ac line cycle VZC areas, where the load condition is much lighter than the peak power delivery and hence PN and PON modes are naturally avoided.

There are several constraints at transition conditions between the stages that help to solve the differential questions. 1) The i_{Lr} and i_{Lm} and v_{cr} should maintain their continuity in the transition from one stage to another. 2) Considering symmetry in the positive and negative half-switching cycles in the steady-state condition, the end values of i_{Lr} and i_{Lm} and v_{cr} are opposite to their initial values. 3) The average output current can be calculated based on the subtraction of the resonant inductor current and magnetizing inductor current during the P or N stage as follows:

$$I_o = \frac{2 \times n}{T_{sw}} \int_0^{T_{sw}/2} (i_{Lr}(t) - i_{Lm}(t))\, dt. \tag{4}$$

The OPO mode in the below resonant frequency area is the light load condition of PO mode and the static dc voltage gain of OPO mode is larger than PO mode. The boundary condition of OPO and PO modes can be found in PO mode. In the boundary PO mode, the v_{Lm} value at the beginning of the P stage should be larger than nV_o to let L_m clamp the output. In order to consider the condition of v_{Lm} at the start of the P stage, the first derivative of the resonant inductor current is calculated at $t = 0$ as i_{Lr} and i_{Lm} reach together at the beginning of the P stage and hence the boundary constraint can be written as

$$\frac{di_{LrP}(0)}{dt} = \left(\frac{1}{Z_r}\right)(V_{in} - nV_o - v_{cr}(0)) = nV_o. \tag{5}$$

Along with the above constraint, the other boundary conditions for PO mode should be written to be able to solve the operation of the boundary of PO and OPO modes. The continuity constraints can be written as follows:

$$\begin{cases} i_{Lr}(0) = i_{Lm}(0) \\ i_{Lr}(t_1) = i_{Lm}(t_1). \end{cases} \tag{6}$$

The symmetry conditions of the half-switching cycle can be written as follows:

$$\begin{cases} i_{Lr}(0) = -i_{Lr}(T_{sw}/2) \\ v_{Cr}(0) = -v_{Cr}(T_{sw}/2). \end{cases} \tag{7}$$

Hence, the unknown parameters of the stage voltage and current equations are as follows, $i_{Lr}(0)$, $i_{Lm}(0)$, t_O, and t_P. If f_{sw} and I_o are given the *LLC* voltage gain M and all the unknowns can be solved for an open-loop condition, and if M and I_o are given f_{sw} and all unknowns can be solved for a closed-loop operation. Fig. 5 illustrates the ac line cycle modeling based

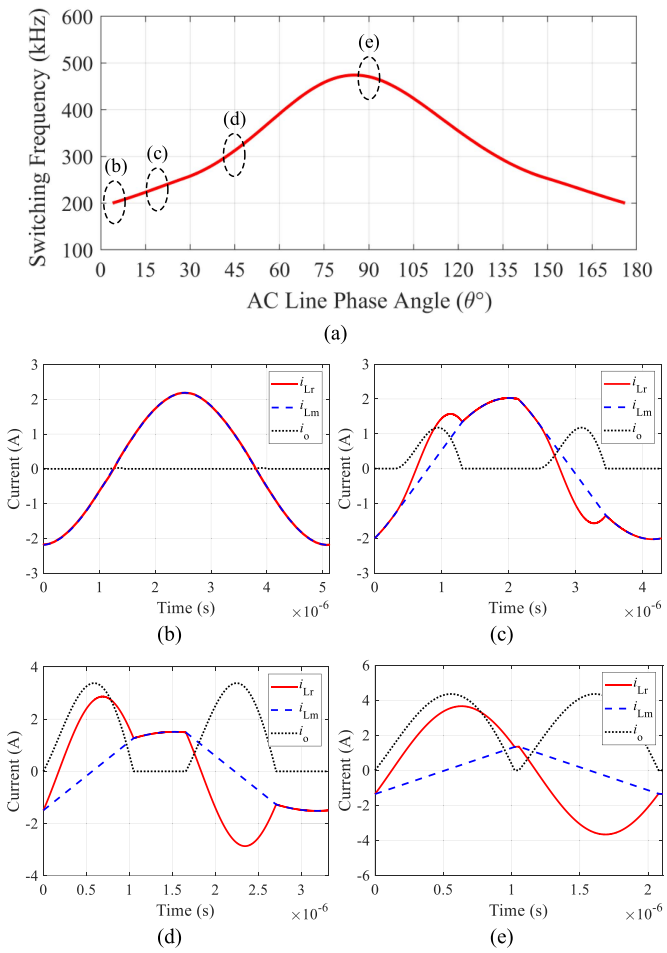

Fig. 5. AC line cycle operation modeling based on time-domain analysis, (a) switching frequency over the AC line half cycle, (b) O mode operation at $\theta = 1°$, (c) OPO mode operation at $\theta = 20°$, (d) PO mode operation at $\theta = 45°$, and (e) PO mode operation at $\theta = 90°$.

TABLE I
GIVEN SPECIFICATIONS

Parameters/Descriptions	Values
Output Power Range (P_o)	330–500 W
ac Voltage (V_{ac})	220 V_{RMS}
Output Voltage Range (V_o)	250–400 V
Line Frequency (f_{line})	50 Hz
Switching Frequency Range (f_{sw})	200–470 kHz
Transformer Turns Ratio (n)	24/19
Magnetizing Inductance (L_m)	120 μH
Resonant Inductance (L_r)	22 μH
Resonant Capacitance (C_r)	4.8 nF
Output Capacitor (C_o)	200 μF

on time-domain analysis and different operating modes that are realized over the ac line cycle for the given specifications listed in Table I. The calculated switching frequency is shown in Fig. 5(a), where the corresponding operating waveforms can be found in Fig. 5(b) to (d). As can be observed from the calculated switching frequency shown in Fig. 5(a) the maximum f_{sw} is happening earlier than $\theta = 90°$ which is because of considering

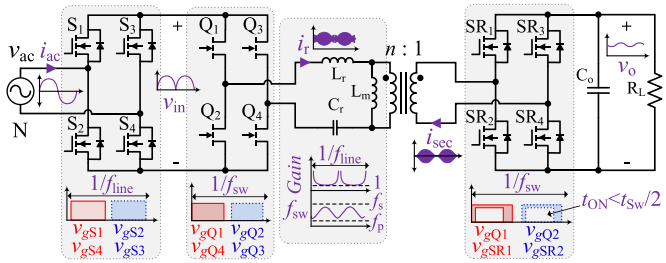

Fig. 6. Single-stage AC–DC LLC converter with input and output synchronous rectifier bridges.

the effect of the output capacitor and output voltage fluctuation in the ac–dc power conversion.

III. Proposed Synchronous Rectification Strategy for AC–DC LLC Converter

Fig. 6 illustrates the structure of a single-stage ac–dc *LLC* converter and some of its main characteristics with active switches for input and output rectifiers over the ac line cycle and switching cycle. The input rectifier bridge switches (S_1-S_4) operate at line frequency (f_{line}) with ZCS performance, which can be implemented with Si MOSFETs. Moreover, the primary side bridge switches (Q_1-Q_4) can take advantage of ZVS that can be implemented with GaN HEMTs, and the secondary side bridge switches (SR_1-SR_4) can take advantage of ZCS that can be implemented with SiC MOSFETs. Using wide bandgap devices allows high switching frequency implementation leading to a high power density design. Since the output rectifier switches of the *LLC* converter should be controlled based on the synchronized pulses with the respective gate pulses of the primary bridge switches, this method is called synchronous rectification. The proper gate pulses for the switching bridges are illustrated in Fig. 6.

Based on the desired operating condition of the *LLC* converter in PFC mode, the majority part of the ac line cycle power delivery is around the peak line voltage while the *LLC* tank is in PO mode providing the highest power to the load. This is then followed by OPO modes at the sides and O modes near the VZC areas, where no power is delivered to the load. It should be mentioned that in a properly designed ac–dc *LLC* converter the O mode normally happens in a very short time; however, if the resonant tank and the inner current loop are not properly designed the O mode can be large. Therefore, to properly control the SRs over the line cycle, it is desired to turn OFF them around VZCs, where no power is delivered to the load to avoid reverse power flow in any O stage. Details of different operating modes over the half ac line cycle with variable frequency primary bridge driving signals and ideal secondary bridge driving signals only operating at the P stage are illustrated in Fig. 7.

From Fig. 7 it can be observed that in the PO mode, the turn ON instant of the SR is synchronized with the respective primary switch with a small turn ON delay (1–2% of the switching cycle) considering the propagation delay of the driver ICs. In OPO mode the turn ON delay of the SRs should be

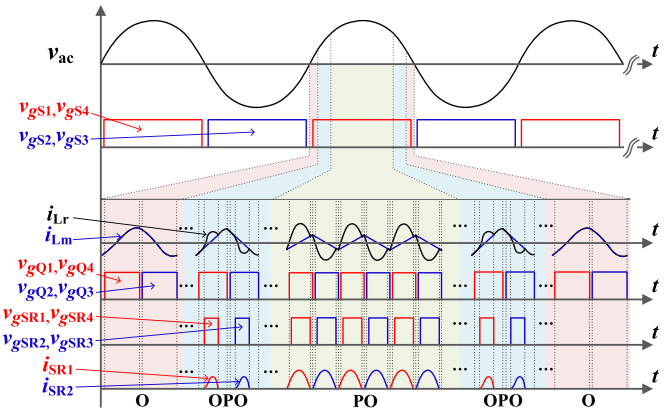

Fig. 7. Different operating modes and respective switching operations over the half AC line cycle.

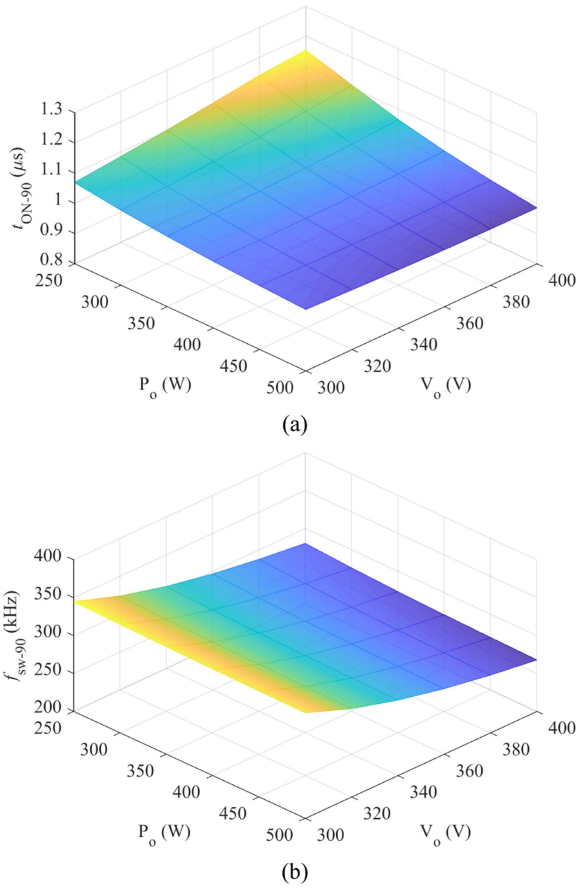

Fig. 8. Time-domain calculation at $\theta = 90°$ for different output voltage and load levels. (a) SR conduction time. (b) Switching frequency.

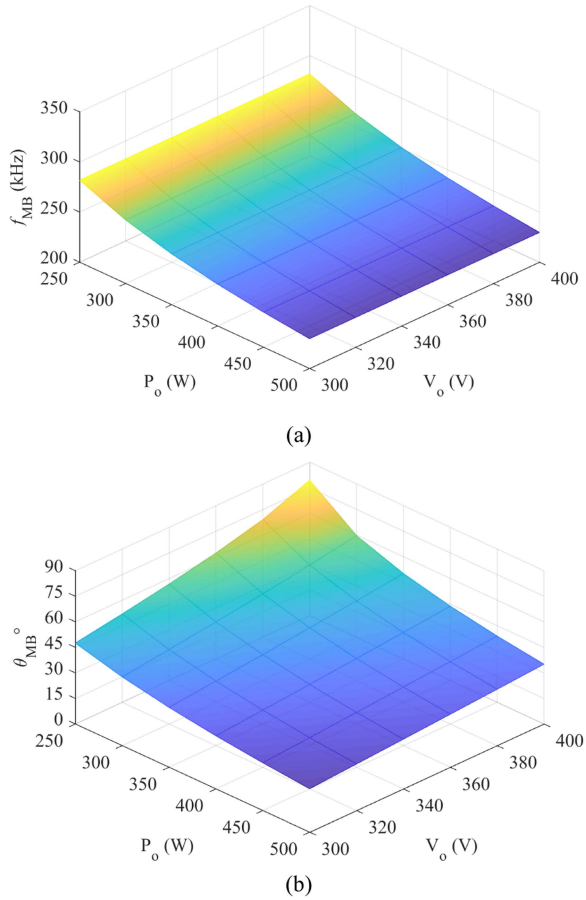

Fig. 9. Time-domain calculation at mode boundary (MB) for different output voltage and load levels. (a) MB switching frequency. (b) MB line phase angle.

adjusted based on the switching frequency and load condition to avoid reverse power flow. Then, the SR conduction time (i.e., equivalent to $t_P \times T_{sw}/2$) that is dependent on the load and switching frequency can be calculated from the time-domain analysis.

The calculated conduction time of the SRs at $\theta = 90°$ (i.e., t_{ON-90}) for different output voltage levels and load conditions is plotted in Fig. 8(a). Moreover, the corresponding peak switching frequency for the same load conditions is plotted in Fig. 8(b). It can be observed that at each output power level, the SR conduction time does not change considerably over the output voltage range at rated output power, and it is more considerable for the half-load condition. Moreover, for the peak switching frequency conditions over the line cycle that are close to the resonant frequency, e.g., for $V_o = 300$ V, the SR conduction time does not change considerably over the load range. From Fig. 8(b) it can be observed that the maximum switching frequency does not change over the load range for a specific output voltage level. Hence, using 3-D look-up tables the SR driving can be implemented based on the calculated conduction and delay times.

In order to simplify the control complexity and use one control variable for SR driving, it is proposed to turn OFF the SRs after the circuit goes into the OPO mode from PO mode to avoid reverse power flow. In this way, as the OPO mode occurs at light load conditions the conversion efficiency does not deteriorate, and the PFC can be realized without any distortion.

The switching frequency at which the mode transition happens (i.e., f_{MB}) can be found from the time-domain analysis by using an additional constrain mentioned in (5), and then the corresponding line phase angle for the mode boundary condition (i.e., θ_{MB}) can be found for every output load condition. Fig. 9

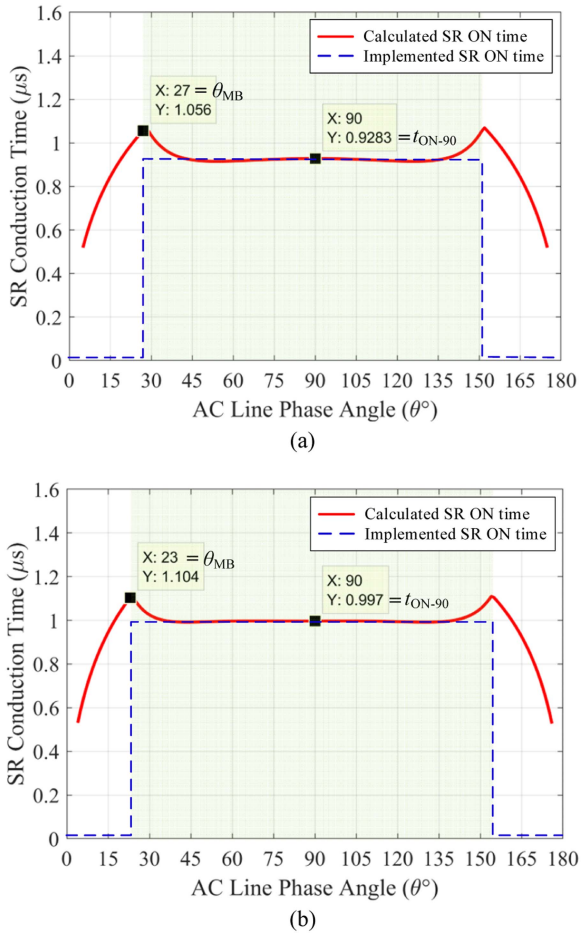

Fig. 10. Calculated SR conduction time at different line phase angles over the AC line half cycle, (a) for $V_o = 400$ V, $P_o = 500$ W, and (b) for $V_o = 250$ V, $P_o = 330$ W.

illustrates the mode boundary switching frequency and line phase angle. From Fig. 9(a) it can be observed that the mode boundary switching frequency is specific to a load level and it is constant over the output voltage variation. However, from Fig. 9(b) it can be observed that over the ac line cycle operation, mode boundary can happen at different line phase angles which is dependent on the output voltage and load levels. Therefore, using a 3-D look-up table based on Fig. 9(b) the line phase angle at which the SRs should start and stop operating over the ac line cycle can be realized.

Fig. 10 illustrates the calculated SR conduction time over the ac line half cycle for two different output voltage and power levels. It can be observed that for the majority of the power delivery the peak power SR conduction time (t_{ON-90}) remains almost unchanged and only below $\theta = 35°$, a noticeable change can be observed in the calculated conduction time. It should be mentioned that the curve peaks in Fig. 10 are related to the instants of transitioning from PO mode to OPO mode and vice versa at θ_{MB} over the line cycle. As the peak SR conduction time at θ_{MB} is only around 10% more than t_{ON-90} and it is happening in a short time at lighter load conditions, to simplify the SR driving strategy and reduce the control implementation complexity, it is proposed to keep the SR conduction time constant until θ_{MB} and turn the SRs OFF for line phase angles below θ_{MB}. The implemented SR operation over the ac half line cycle is illustrated with a blue dashed line in Fig. 10. It should be mentioned that here the circuit parameters are tuned such that the effect of the parasitic components of a real circuit is considered and the calculated values are more similar to that of the experimental implementation.

Hence, in the proposed SR driving strategy, the SRs are turned ON with a fixed calculated ON time for the PO mode and they are turned OFF soon after the circuit starts operating in the OPO mode. In this way, the majority of the ac power is delivered to the load when SRs are operating. This method improves efficiency over using a fixed conduction time of the SRs for every load condition by totally avoiding reverse power flow in the O stages and its simplicity allows implementation with any low-cost MCU.

As the operation of the resonant converters is highly dependent on the resonant tank components, it is crucial to investigate the effect of the component tolerances on the calculated SR conduction time over the ac line cycle. As inductor manufacturing tolerance is less controllable compared with the capacitor tolerance, it is reasonable to consider a 10% tolerance for the resonant inductors and consider a 5% tolerance for the resonant capacitor. Fig. 11 illustrates the calculated SR conduction time over the ac line cycle for 400-V output voltage condition considering resonant tank component tolerances. From Fig. 11 it can be observed that with 10% tolerance in the resonant inductor, less than 5% tolerance in the calculated SR conduction time can be observed (i.e., <50 ns). Moreover, with 5% tolerance in the resonant capacitor around 2% tolerance is observed in SR conduction time (i.e., <25 ns). It can be observed that the effect of magnetizing tolerance is much less than the effect of the tolerances of the series resonant components. Moreover, increased series resonant component value increased the SR conduction time, and increased magnetizing inductor reduces the SR conduction time. Fig. 12 illustrates the SR conduction time for $V_o = 250$ V. A similar behavior can be observed here while the effect of magnetizing inductor tolerance is negligible for $V_o = 250$ V which is because around the ac peak the operation remains close to the series resonant frequency that has less dependency on the resonant tank impedance. Hence, it can be concluded that the proposed SR driving strategy can be reliably implemented over the ac line cycle considering reasonable resonant tank component tolerances.

Fig. 13 illustrates the digital control implementation of the proposed SR driving strategy using 3-D look-up tables for the line cycle turn OFF angle using the mode boundary line angle similar to Fig. 9(b) and calculated SR conduction time similar to Fig. 8(a). It should be mentioned that the line angle information in combination with θ_{MB} is used to turn ON/OFF the SRs over the ac line cycle. The primary bridge is driven based on frequency modulation using the output of the outer voltage and inner current loops. Then the SRs are synchronized to the primary bridge gate signals and driven with duty cycle modulation using t_{ON}. Moreover, low-frequency input rectification can be done using the I/O module of the MCU. It is worth mentioning that

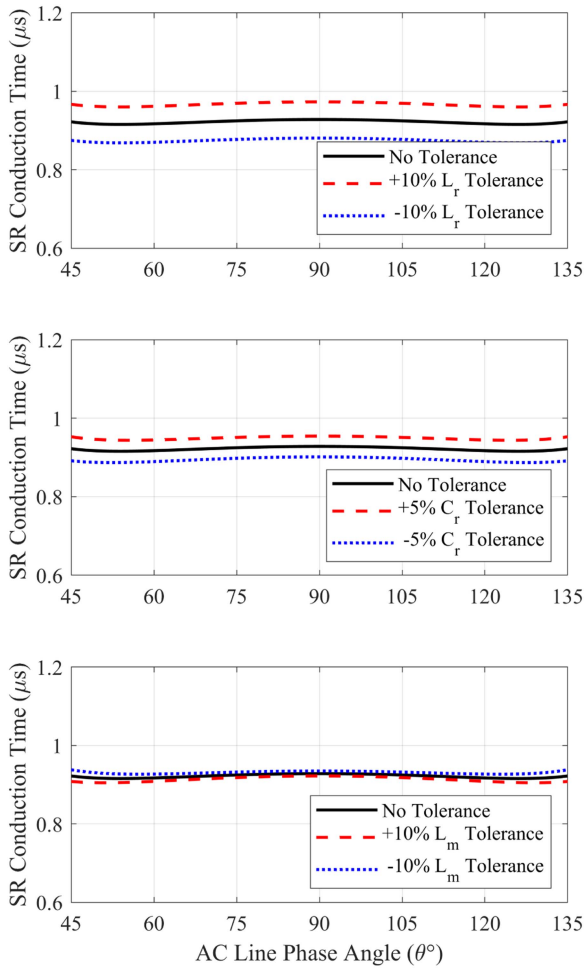

Fig. 11. Calculated SR conduction time considering resonant tank component tolerances for $V_o = 400$ V.

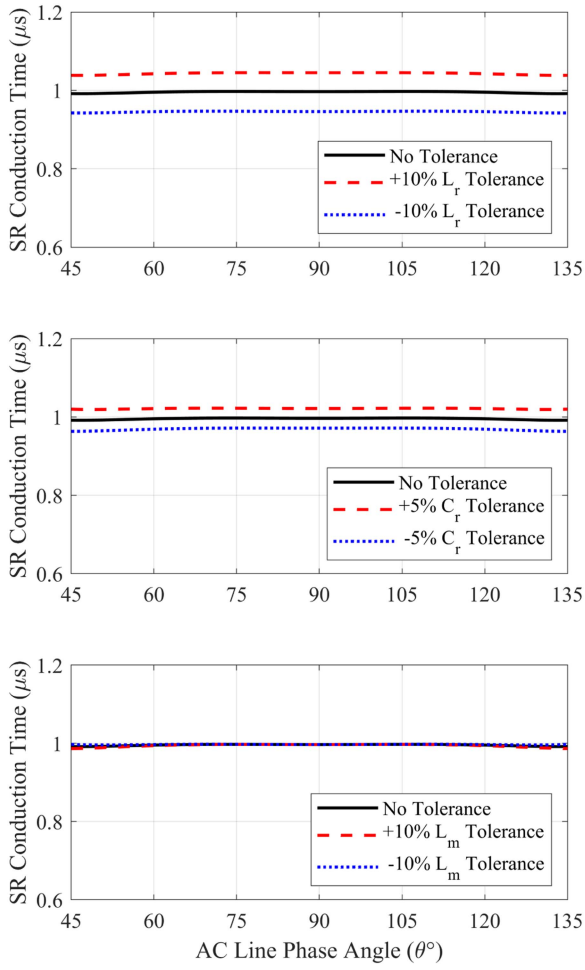

Fig. 12. Calculated SR conduction time considering resonant tank component tolerances for $V_o = 250$ V.

based on Fig. 10 as the calculated SR conduction time has less than 10% variation in the PO mode operation over the ac line cycle it is possible to use a fixed conduction time for simplicity.

IV. Experimental Validation

A scaled-down laboratory prototype is built using wide bandgap semiconductors (i.e., GaN and SiC) to verify the performance of the proposed SR driving strategy for single-stage ac–dc *LLC* converters. The main components used in the laboratory prototype are listed in Table II. A picture of the laboratory prototype is shown in Fig. 14. A low-cost microchip dsPIC microcontroller is used to implement pulse frequency modulated control and perform PFC by providing proper driving signals over the ac line cycle for all the switching bridges of the single-stage ac–dc *LLC* converter. It should be mentioned that input diode rectifiers are 650-V Si MOSFETs and 650-V GaN HEMTs are used for the primary switching bridge, while 650-V SiC MOSFETS are used for the SRs. Different scenarios are implemented in practice for the sake of comparison. First,

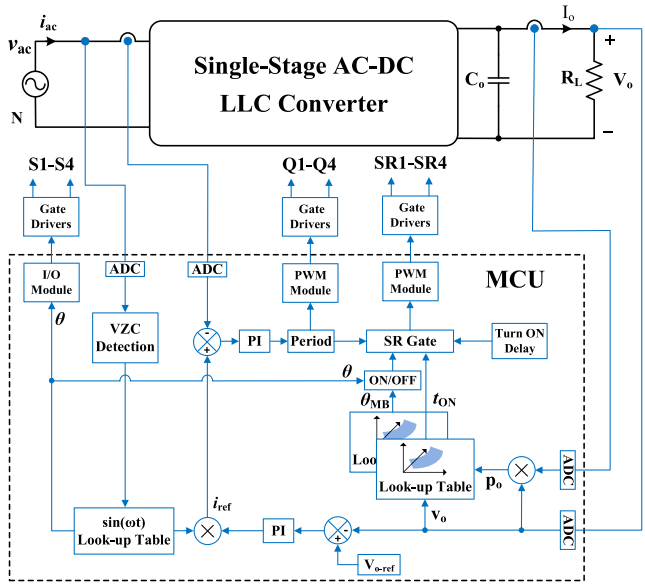

Fig. 13. Digital implementation of the proposed SR driving strategy for the single-stage AC–DC LLC converter.

TABLE II
MAIN COMPONENTS USED IN THE PROTOTYPE

Parameters/Descriptions	Values
Magnetizing Inductor (L_m)	120 μH (PQ3230 - 3F36)
Resonant Inductor (L_r)	23 μH (PQ2620 - 3F36)
Input Rectifier Bridge Si MOSFET	IPP60R099P7 (650 V–31 A–99 mΩ)
Inverter Bridge GaN E-HEMT	GS66504B (650 V–15A–130mΩ)
Output Rectifier Bridge SiC MOSFET	C3M0120065J (650 V– 21 A–157 mΩ)

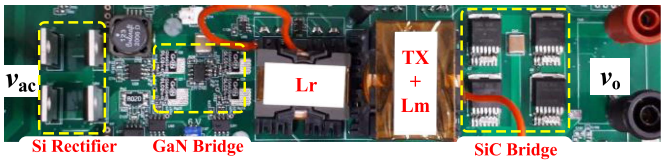

Fig. 14. Picture of the scaled-down AC–DC LLC converter laboratory prototype.

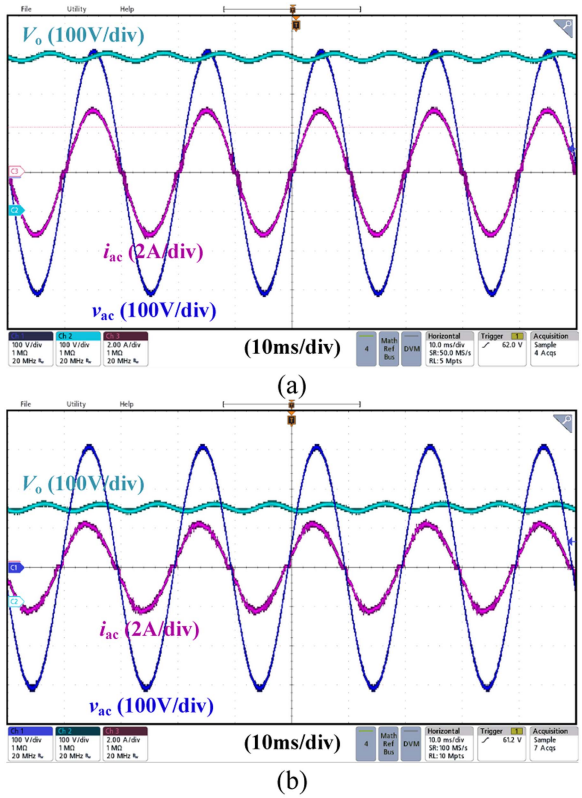

Fig. 15. Experimental results of the single-stage AC–DC LLC converter for (a) $V_o = 400$ V, $P_o = 500$W, and (b) $V_o = 250$ V, $P_o = 330$ W.

the SR is switched with a fixed conduction time found from the calculation. Second, the proposed method is implemented by turning ON and OFF the SRs over the ac line cycle based on the θ_{MB} that is found from the time-domain calculation. Last, an adaptive SR driving is implemented using look-up tables mapped for both the turn ON delay and SR conduction time for

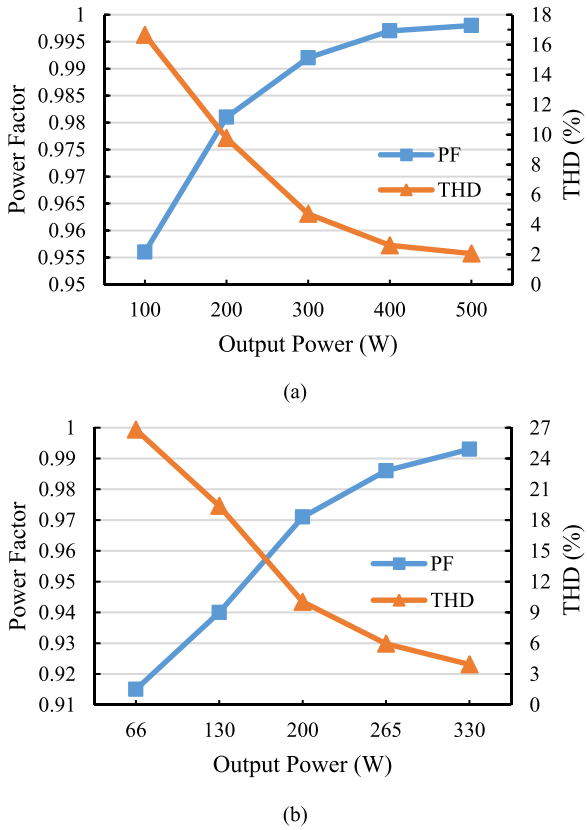

Fig. 16. Measured power factor and THD over the load range for (a) $V_o = 400$ V, and (b) $V_o = 250$ V.

different load levels to compare the efficiency with the proposed SR driving method.

The proper PFC operation of the implemented prototype is shown in Fig. 15 for both output voltage conditions. As can be observed the input current is sinusoidal with a high-power factor (PF) and low total harmonic distortion (THD). Moreover, the measured PF and THD over the load range for both output voltage conditions are shown in Fig. 16. It can be observed that the worst-case PF in light load is more than 0.9 and the full load THD is less than 5% for both cases. It should be mentioned that if a lower THD is required for light load operation a line cycle skipping method can be implemented, as suggested in [37].

Fig. 17(a) shows the experimental result of the single-stage ac–dc *LLC* converter with a fixed SR ON time over the ac line cycle. As can be observed around the VZC points the *LLC* converter operates in O and OPO modes, and hence by modulating SRs in that area some reverse power flow is introduced which decreases the power conversion efficiency over the ac line cycle. Zoomed-in waveforms at $\theta = 24°$, $\theta = 20°$, and $\theta = 10°$ are shown in Fig. 17(b)–(d), respectively. The reverse current due to early turn ON of the SRs can be observed in all OPO conditions in the secondary current waveform which is more severe in smaller ac line phase angles.

The experimental result with the proposed SR driving strategy for $V_o = 400$ V is shown in Fig. 18, where the SRs are turned ON after $\theta = 26°$ to avoid reverse power transfer in OPO and

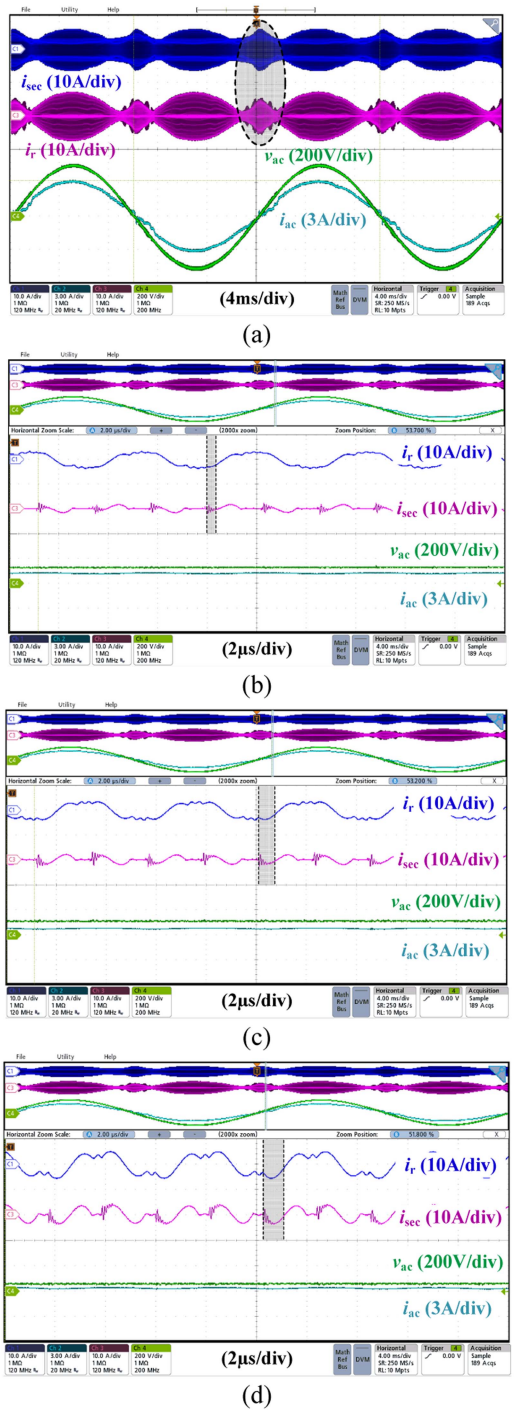

Fig. 17. Experimental results using a fixed SR ON time over the line cycle for (a) $V_o = 400$ V, $P_o = 500$ W, (b) $V_{in} = 125$ V, $\theta = 24°$, (c) $V_{in} = 105$ V, $\theta = 20°$, and (d) $V_{in} = 55$ V, $\theta = 10°$.

O modes. From Fig. 18(b)–(d) it can be observed that a fixed conduction time of 940 ns is providing a proper turn ON and OFF instants for the SRs. Below $\theta = 26°$ the turn ON delay starts to become larger and hence the SRs are turned OFF after that phase angle to avoid reverse current flow. The conduction time and the mode boundary line phase angle are according to Fig. 10(a) which is based on the time-domain calculation. In Fig. 18(e) and

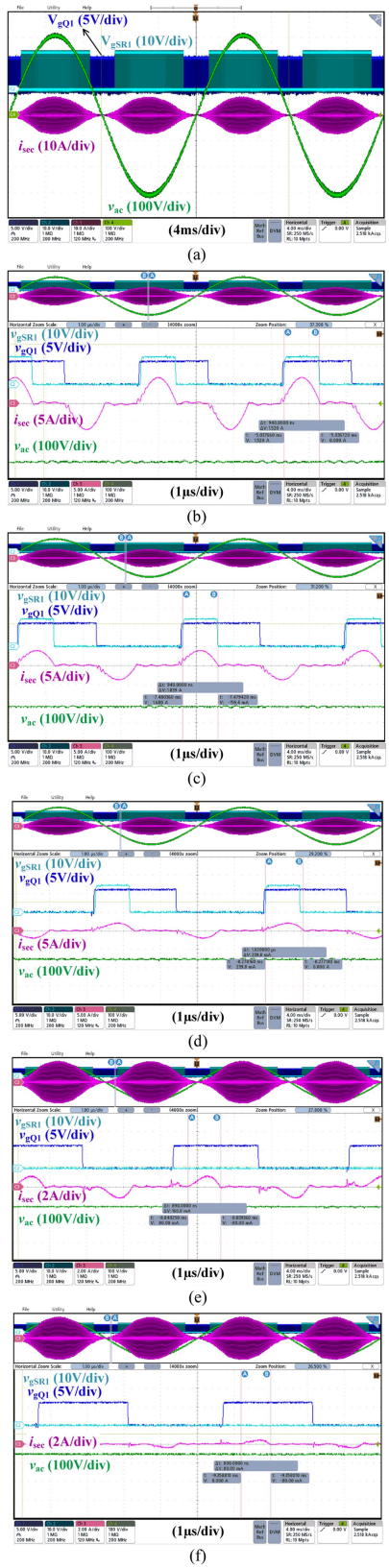

Fig. 18. Experimental results of the proposed AC line cycle SR driving strategy for (a) $V_o = 400$ V, $P_o = 500$ W, (b) $V_{in} = 311$ V, $\theta = 90°$, $t_{ON} = 940$ ns, (c) $V_{in} = 220$ V, $\theta = 45°$, $t_{ON} = 940$ ns, (d) $V_{in} = 155$ V, $\theta = 30°$, $t_{ON} = 940$ ns, (e) $V_{in} = 105$ V, $\theta = 20°$, $t_{ON} = 890$ ns, and (f) $V_{in} = 55$ V, $\theta = 10°$, $t_{ON} = 800$ ns.

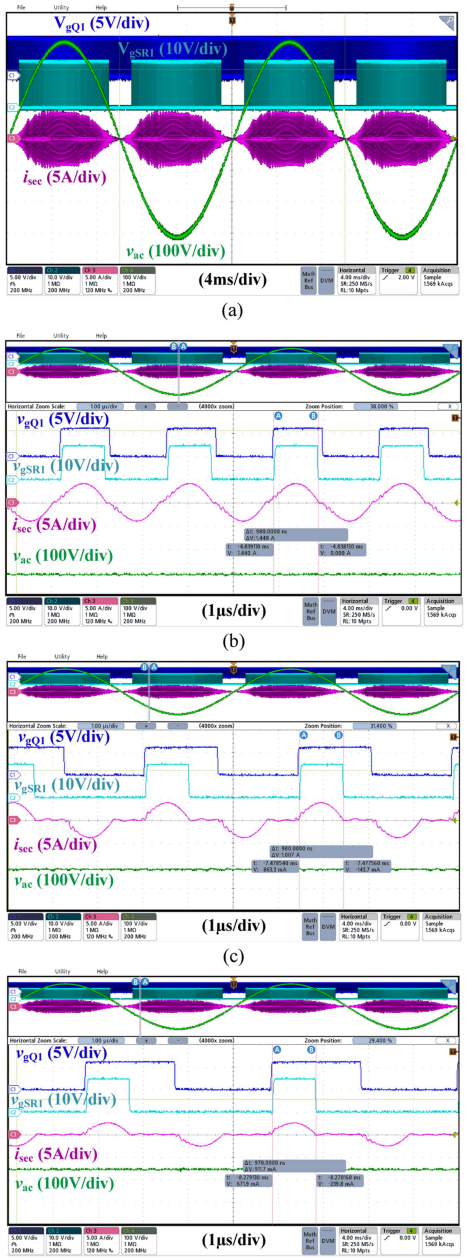

Fig. 19. Experimental results of the proposed AC line cycle SR driving strategy for (a) $V_o = 250$ V, $P_o = 330$ W, (b) $V_{in} = 311$ V, $\theta = 90°$, $t_{ON} = 980$ ns, (c) $V_{in} = 220$ V, $\theta = 45°$, $t_{ON} = 980$ ns, (d) $V_{in} = 155$ V, $\theta = 30°$, $t_{ON} = 970$ ns.

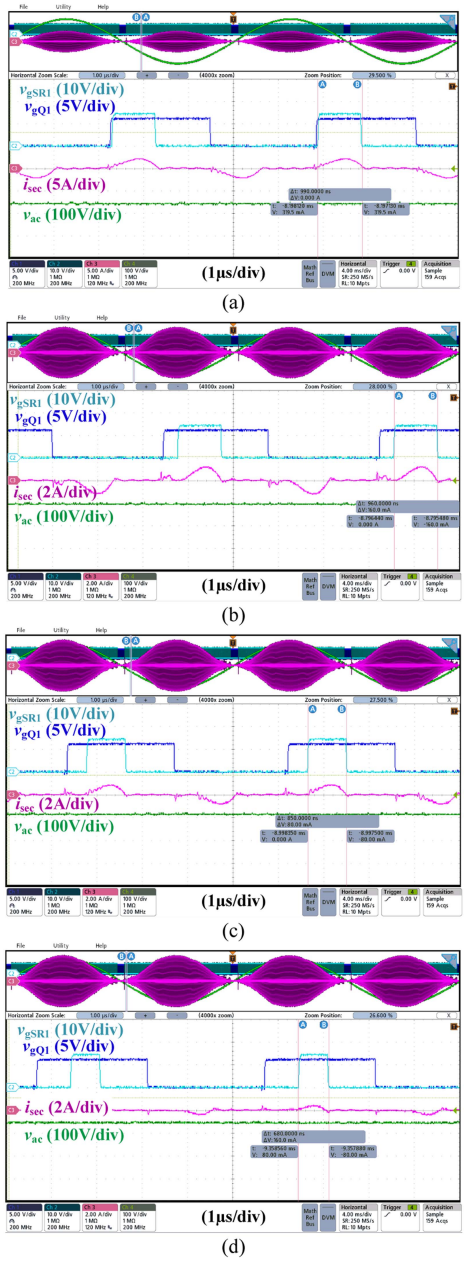

Fig. 20. Experimental results of an adaptive SR driving approach for the OPO mode of operation for $V_o = 400$ V, $P_o = 500$ W, (a) $V_{in} = 155$ V, $\theta = 30°$, $t_{ON} = 990$ ns, (b) $V_{in} = 105$ V, $\theta = 20°$, $t_{ON} = 960$ ns, (c) $V_{in} = 85$ V, $\theta = 15°$, $t_{ON} = 850$ ns, and (d) $V_{in} = 55$ V, $\theta = 10°$, $t_{ON} = 680$ ns.

(f), the operating conditions at $\theta = 20°$ and $\theta = 10°$ are shown, respectively. It can be observed that there is no reverse current flow as the body diode of the SiC MOSFETs are fast enough and hence operating properly.

Fig. 19 illustrates the proposed SR driving strategy for $V_o = 250$ V and $P_o = 330$ W condition. Due to brevity only three operating conditions at $\theta = 90°$, $\theta = 45°$, and $\theta = 30°$ are shown in Fig. 19(b)–(d), respectively. In this condition, a fixed conduction time of 980 ns is used from $\theta = 90°$ down to $\theta = 24°$ to avoid reverse current flow in OPO mode. The calculated conduction time and the mode boundary shown in Fig. 10(b) are in accordance with the experimental results illustrated in Fig. 19.

Furthermore, to emulate an online SR tuning over the ac line cycle an adaptive SR driving for turn ON delay and conduction time is implemented via look-up tables using the calculated values found from the time-domain analysis to compare the efficiency with the proposed SR driving method. Only the OPO mode part of the operation for $V_o = 400$ V, $P_o = 500$ W condition with an adaptive turn ON delay and conduction time is illustrated in Fig. 20. It can be observed that there is no reverse current in OPO mode, and the SRs are turned ON and OFF at the right time. Moreover, it is found that the efficiency with the complicated

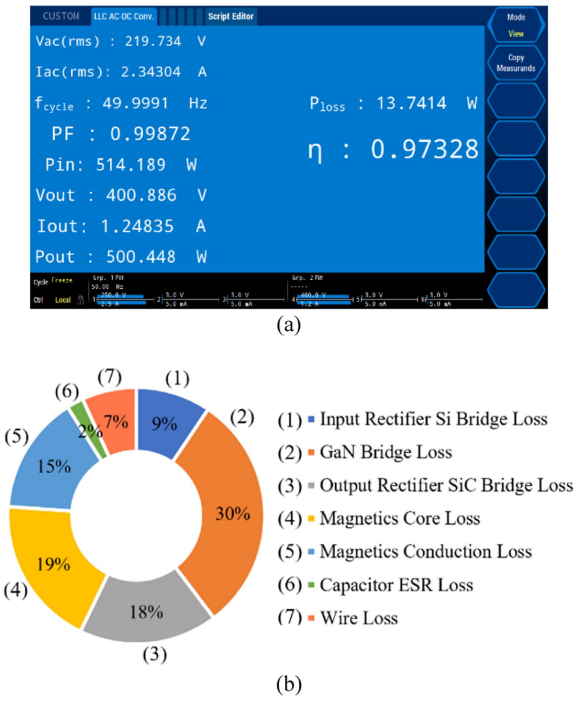

Fig. 21. Efficiency and loss of the AC–DC LLC converter with the proposed SR driving strategy for $V_o = 400$ V, (a) power analyzer output, and (b) calculated power loss breakdown.

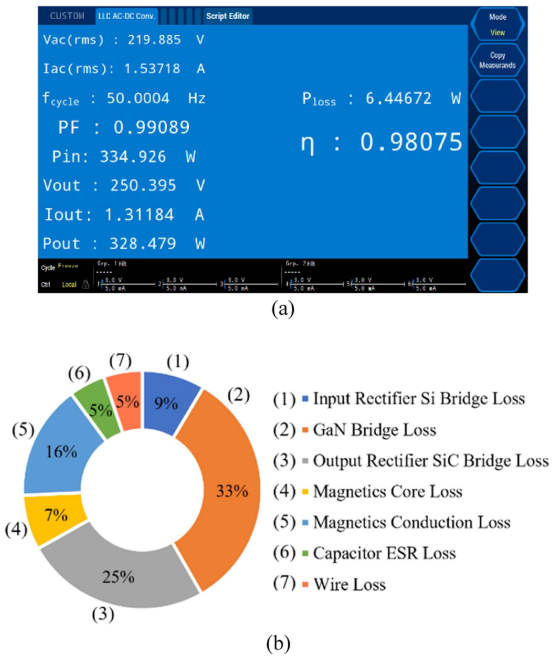

Fig. 22. Efficiency and loss of the AC–DC LLC converter with the proposed SR driving strategy for $V_o = 250$ V, (a) power analyzer output, and (b) calculated power loss breakdown.

online tuning SR driving will either be similar to or less than 0.1% higher than the proposed simple SR driving strategy.

Fig. 21(a) illustrates the full load efficiency of 97.3% that is achieved for $V_o = 400$ V at $I_o = 1.25$ A (i.e., $P_o = 500$ W) condition which is 0.8% higher than using a fixed SR conduction time over the ac line cycle. The estimated power loss breakdown for this condition is shown in Fig. 21(b). The peak efficiency for $V_o = 250$ V at $I_o = 1.3$ A (i.e., $P_o = 330$ W) condition was measured to be 98.1% which is shown in Fig. 22(a). For the same load condition, the efficiency of the case with a fixed SR conduction time is 0.5% lower. The power loss breakdown for this condition is shown in Fig. 22(b). It should be mentioned that all the efficiency measurements are carried out using an LMG671 Zimmer precision power analyzer. It can be observed that a high power factor of more than 0.99 is achieved over the output voltage range while achieving a high conversion efficiency. The main reasons for the larger efficiency drop for $V_o = 400$ V is because of higher derating of the output decoupling capacitor and higher magnetics losses. Moreover, the operation for this output voltage is at a lower frequency range far away from the series resonant frequency where the circulating current is larger at the primary side of the transformer.

The efficiency curves at different output load levels using the proposed SR driving method and using a fixed SR conduction time are depicted in Fig. 23. It can be observed that using the proposed SR driving strategy the efficiency is significantly improved over the fixed SR turn ON time and the improvement is more at lighter load conditions than full-load conditions. The main reason that the efficiency difference in Fig. 23(a) is larger than in Fig. 23(b) is that the O mode in the OPO mode for the 400-V output voltage condition is longer than the 250-V condition which introduces more reverse current in OPO modes in case of using a fixed SR ON time and hence introduces more conduction losses.

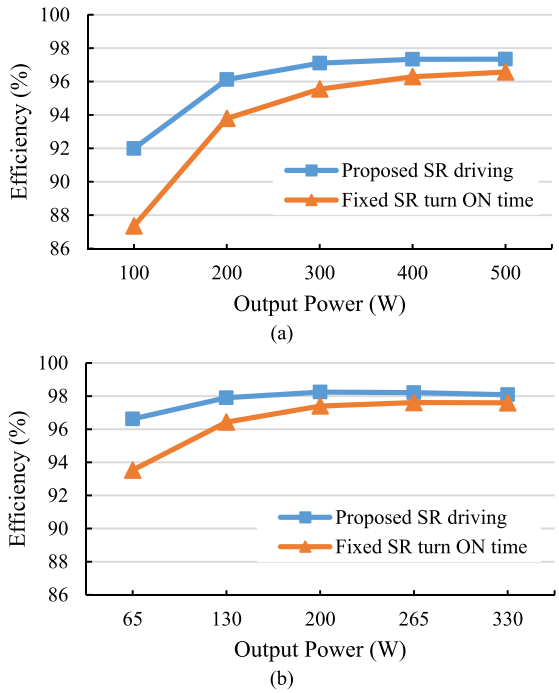

Fig. 23. Efficiency curves of the AC–DC LLC converter using both the proposed synchronous rectification and a fixed SR conduction time for (a) $V_o = 400$ V, and (b) $V_o = 250$ V.

V. Conclusion

This article proposed a simple synchronous rectification strategy for single-stage ac–dc *LLC* converters that is based on generating the driving signals in the MCU. The ease of implementation and effectiveness of the proposed method is a key feature that allows reliable efficiency improvement via proper SR operation for high power and high output voltage applications above 200 V. The principles of operation and analysis of the proposed SR driving strategy based on the time-domain analysis show that a single control variable based on the SR conduction time can be used over the ac line cycle for every output load condition. Experimental results verified the analysis and the efficacy of the proposed SR driving strategy for different output voltage and load conditions. Maximum efficiency of 98.1% is achieved using the proposed method showing a 0.5% improvement over using a fixed conduction time over the ac line cycle. Furthermore, the experimental results show that the conversion efficiency is either similar or only 0.1% less than a more complex adaptive method with multiple control variables.

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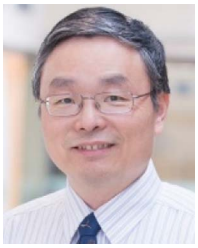

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