Complementary Couple-Turns: An Effective Method for Reducing Common-Mode Noise in Full-Bridge *LLC* Resonant Converter with Split Primary Winding Transformer

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***Abstract*—In conventional Full-Bridge (FB) *LLC* resonant converters, the position of the resonant tank can affect the symmetry of the entire circuit, leading to different *dv/dt* values at the two winding terminals of the transformer. This results in non-cancelable displacement currents generated in the parasitic interwinding capacitance of the transformer, leading to severe Common-Mode (CM) noise issues. In this paper, a low CM noise FB *LLC* resonant converter with the Split Primary Winding Transformer (SPWT) configuration is proposed. The transformer primary winding is split into two windings and the resonant tank is connected between these two windings. With a symmetrical winding structure, the CM noise current generated in the transformer can be canceled completely. The concept of complementary couple-turns is proposed to ensure a symmetrical winding arrangement for the planar transformer in the Printed Circuit Board (PCB) layout stage before it is fabricated physically. Practical considerations have been discussed when implementing the SPWT configuration, including leakage inductance, transformer winding loss, and voltage conversion ratio. A 360 W FB *LLC* converter with planar transformers is built to verify the proposed methods.**

***Index Terms*—Split Primary Winding Transformer (SPWT), Full-Bridge (FB), *LLC* resonant converter, Common-Mode (CM) noise, Planar transformer.**

I. Introduction

COMMON-MODE (CM) noise primarily arises from the displacement currents flowing through parasitic capacitors with high *dv/dt* nodes, which can disrupt the proper functioning of electronic devices, equipment, and systems [1]. CM filters, which include Y-capacitors and bulky CM inductors, are usually employed to ensure that power converters meet the corresponding Electromagnetic Interference (EMI) standards. To improve the power density of the overall system, it is important to achieve low CM emissions of power converters so as to shrink the size of CM filters [2].

The Full-Bridge (FB) *LLC* resonant converter has been widely used in medium-to-high power applications because of its simple structure, high cost-effectiveness, and soft-switching capability [3]-[5]. The FB *LLC* converter possesses a natural symmetrical structure, which yields a pair of switching nodes having complementary electric potentials with respect to the ground. When the associated parasitic capacitances of these nodes are equal, the generated CM noise displacement currents can be completely canceled by each other. However, the voltage across the resonant tank affects the electric potentials of the transformer's primary winding terminals, which generates a large CM noise displacement current in the interwinding capacitance of the transformer [6]. This issue is particularly severe in planar transformers, which have a larger parasitic interwinding capacitance than traditional wire-wound transformers due to the larger overlapping area between adjacent winding layers [7]-[9]. The combination of large parasitic interwinding capacitance and large *dv/dt* difference leads to severe CM noise problems.

Various methods have been proposed to suppress the CM noise current flowing through the transformer of isolated power converters [10]-[26]. The shielding technique is widely used to block the electric coupling between the transformer primary and secondary windings [10]-[14]. However, there is a large conduction loss in shielding layers because of the eddy current, which results in lower converter efficiency. In [15]-[17], the overlapping primary and secondary winding layers of the transformer are made to have the same voltage distributions. There is no CM noise displacement current in the interwinding capacitance because of zero *dv/dt*. But this approach does not work for FB *LLC* converters since there are no static points in transformer primary winding terminals. The CM noise current cannot be completely canceled. In [18], a static-point connection is proposed to establish the static points at the primary winding, so as to build the paired winding layers with the same *dv/dt*. However, it is hard to implement this approach in medium-to-high power applications with planar transformers. Especially for the high turns ratio planar transformer with an interleaved winding structure, too many paired layers are needed to maintain zero *dv/dt* between primary and secondary winding layers, which results in high manufacture cost and large transformer size. Passive components and extra transformer winding can be used to cancel the CM noise current in [19]-[26]. In [19]-[22], balanced resonant tanks are utilized for the CM noise reduction of FB *LLC* converters. Each resonant inductor and capacitor are separated into two components with the same value. The balance condition is sensitive to the components' tolerance. CM noise cancellation capacitor is added to the transformer in [23]-[25]. The capacitor value is selected based on the calculation or experimental results of the transformer's equivalent interwinding capacitance. In [26], an antiphase winding is introduced to generate the out-of-phase CM noise current. Although the CM noise performance can be improved, extra components or transformer windings are needed which

increases the cost and decreases the power density of the converter.

A method of balanced windings has been proposed in [27] for flyback converters. This method divides the primary winding of the flyback transformer into two branches, with the switch and control logic branch placed in the middle. However, the approach discussed in [27] is based on wire-wound transformers and does not provide a universally applicable winding method for transformers. In this paper, the concept of balanced windings is extended to the FB *LLC* converter to reduce the CM noise. The *LLC* transformer primary winding is split into two windings and the resonant tank is connected between these two windings. The split primary windings of the transformer are wound on the same magnetic core. This FB *LLC* configuration is first mentioned in this paper, which is named as Split Primary Winding Transformer (SPWT). The equivalent CM noise circuit of the FB *LLC* converter with SPWT configuration is developed and analyzed in detail. It has been found that, with a symmetrical winding structure, the CM noise current generated in the transformer can be canceled completely. The symmetrical conditions of the transformer from the CM noise perspective are discussed, and the concept of complementary couple-turns is proposed to ensure a symmetrical winding structure for the planar transformer. The proposed complementary couple-turns offers a simple and cost-effective solution for reducing CM noise in the SPWT configuration based FB *LLC* converter without using any additional components.

This paper is organized as follows: Section II provides an analysis of CM noise in conventional FB *LLC* converters, which reveals that the different *dv/dt* characteristics of transformer primary winding terminals lead to non-cancelable CM noise currents, resulting in degraded CM EMI performance. Section III presents the SPWT configuration for the FB *LLC* converter and develops a CM noise model, which demonstrates that the CM noise in the transformer with SPWT configuration can be canceled completely by ensuring a symmetrical winding arrangement. In section IV, the concept of complementary couple-turns is proposed to ensure a symmetrical winding arrangement for the planar transformer. Section V discusses the influences of SPWT configuration on the FB *LLC* converter, including transformer leakage inductance, transformer winding loss, and voltage conversion ratio. Section VI presents experimental verification, and Section VII concludes the paper.

II. CM Noise Analysis of Conventional FB *LLC* Resonant Converter

Fig. 1 depicts the CM noise propagation paths of the conventional FB *LLC* converter. During the conducted EMI measurement, the secondary ground (SG) is connected to the protective earth (PE). The CM noise currents generated by the switching nodes will couple into the PE via parasitic capacitances, which can be detected by the line impedance stabilization network (LISN). The LISN, as a passive network, serves the purpose of isolating the testing system with a

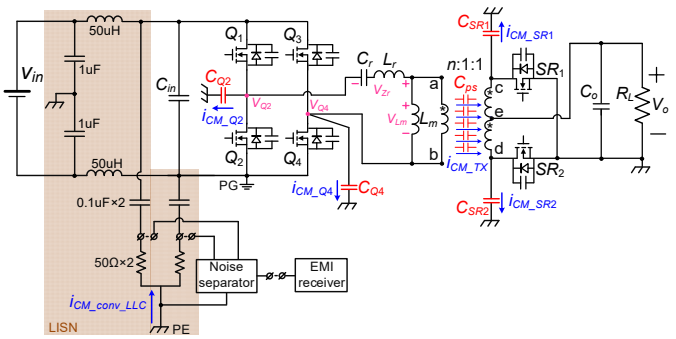


Fig. 1. CM noise propagation paths of conventional FB *LLC* resonant converter.

reference impedance and providing measurement points to the EMI receiver. A noise separator is utilized to effectively separate the original conducted EMI noise into its CM noise component.

As shown in Fig. 1, on the secondary side, i_{CM_SR1} and i_{CM_SR2} denote the CM noise currents generated by the secondary-side voltage pulsation nodes on the circuit-to-PE parasitic capacitors (C_{SR1} and C_{SR2}). Since SG is connected to PE, they circulate back through SG instead of LISN. Hence, i_{CM_SR1} and i_{CM_SR2} do not contribute to the total CM noise and can be ignored.

Typically, the magnitude of the current passing through the LISN is in the range of microamperes to milliamperes. In particular, a CM current of 40 μA at 150 kHz (which translates to 66 dBμV when flowing into 50 Ω) exceeds the limits specified by EN55032 Class B (quasi-peak value). Therefore, the *dv/dt* of the LISN can be considered negligible compared to that of the converter's voltage pulsation nodes, and the primary ground (PG) can be treated as equivalently connected to PE from the perspective of CM noise coupling. On the primary side, C_{Q2} (C_{Q4}) is the parasitic capacitor between the drain of MOSFET Q_2 (Q_4) and PE. By using PE as the reference point, the electric potentials of primary phase-leg midpoints are denoted by v_{Q2} and v_{Q4}. The CM noise currents generated in C_{Q2} and C_{Q4} are denoted by i_{CM_Q2} and i_{CM_Q4}, respectively. Given the symmetrical layouts of the two primary phase legs and the consistent packaging of the MOSFETs, C_{Q2} can be considered as equal to C_{Q4}. Since Q_2 and Q_4 are switched at 50% duty and 180 degrees out of phase with each other, v_{Q2} and v_{Q4} have complimentary *dv/dt* characteristics. When v_{Q2} has a positive *dv/dt*, v_{Q4} will have a negative *dv/dt* with the same amplitude. Therefore, i_{CM_Q2} and i_{CM_Q4} will be canceled by each other. i_{CM_Q2} and i_{CM_Q4} are removed from the following CM noise analysis.

According to the above analysis, the total CM noise current $i_{CM\_conv\_LLC}$ is dominated by i_{CM_TX}. i_{CM_TX} represents the total CM noise displacement current flowing through the distributed interwinding capacitance C_{ps} of the transformer. i_{CM_TX} is related to the electric potentials of the transformer winding terminals and parasitic interwinding capacitance of the transformer. In order to quantitatively analyze i_{CM_TX}, the parasitic interwinding capacitance model of the transformer has been developed. By ignoring the effect of the transformer's

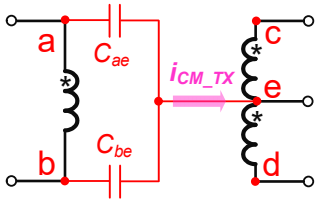


Fig. 2. Lumped interwinding capacitance mode of transformer in conventional FB *LLC* resonant converter.

leakage inductance, the two-capacitor model can be used to characterize the interwinding capacitance of a center-tapped three-winding transformer [24]. As shown in Fig. 2, C_{ae} and C_{be} are used to model the lumped interwinding capacitors of the transformer. Since the winding terminal *e* is connected to the dc output, the corresponding *dv/dt* can be treated as zero. Thus, i_{CM_TX} can be calculated by (1), where v_a and v_b denote the electric potentials of transformer primary winding terminals *a* and *b* with respect to PE. When a transformer is constructed, the values of C_{ae} and C_{be} are then determined. v_a and v_b will vary with different operation conditions of the *LLC* converter, and then influence the CM EMI performance of the whole system.

$$i_{CM\_TX} = C_{ae}\frac{dv_a}{dt} + C_{be}\frac{dv_b}{dt} \tag{1}$$

In Fig. 1, since the winding terminal *b* is connected to the drain of MOSFET Q_4, v_b is consistent with v_{Q4} which is a typical trapezoidal wave. v_a is equal to v_{Q2} + v_{Zr}, where v_{Zr} denotes the voltage across the resonant tank. So, (1) can be rewritten as shown in (2), where dv_{Q2}/dt is substituted by -dv_{Q4}/dt since v_{Q2} and v_{Q4} have complementary *dv/dt* characteristics. If the transformer is made symmetrically, the values of C_{ae} and C_{be} can be treated as equal; then the influence of dv_{Q4}/dt on i_{CM_TX} can be eliminated. However, the influence of v_{Zr} still exists.

$$\begin{aligned} i_{CM\_TX} &= C_{ae}\frac{d(v_{Q2}+v_{Zr})}{dt} + C_{be}\frac{dv_{Q4}}{dt} \\ &= (C_{be}-C_{ae})\frac{dv_{Q4}}{dt} + C_{ae}\frac{dv_{v_{Zr}}}{dt} \end{aligned} \tag{2}$$

In conclusion, the placement of the resonant tank between the midpoint of the primary phase leg and transformer winding terminal *a* introduces an additional CM noise voltage variable, v_{Zr}. v_a and v_b will exhibit different *dv/dt* characteristics because of the influence of v_{Zr}. The CM noise displacement currents generated by v_a and v_b cannot be canceled with a symmetrical transformer winding arrangement. And CM noise is not minimized. In order to reduce the CM noise in the conventional FB *LLC* converter, the displacement currents generated by v_a and v_b via the corresponding parasitic interwinding capacitors should be eliminated.

III. SPWT Configuration for FB *LLC* Resonant Converter

Fig. 3 shows the circuit diagram of the FB *LLC* converter with the SPWT configuration. Compared to conventional FB *LLC* converters, the transformer's primary winding is split into

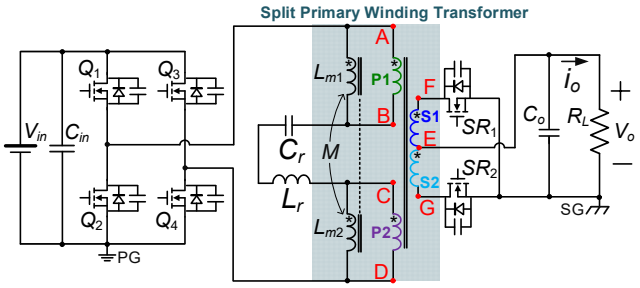


Fig. 3. FB *LLC* resonant converter with SPWT configuration.

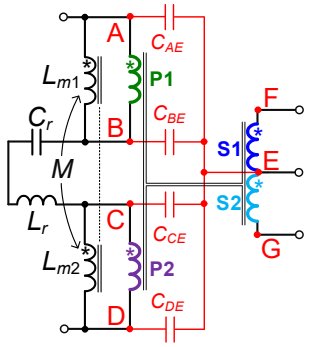


Fig. 4. Lumped interwinding capacitance model of transformer in proposed FB *LLC* resonant converter.

two separate windings *P*1 and *P*2. The split two primary windings *P*1 and *P*2 have the same number of turns. The resonant inductor L_r and resonant capacitor C_r are placed between the primary windings *P*1 and *P*2. L_{m1} (L_{m2}) denotes the magnetizing inductance seen from the primary winding *P*1 (*P*2). *M* denotes the mutual inductance of L_{m1} and L_{m2}. The total primary side magnetizing inductance L_{m_SPWT} is calculated as

$$L_{m\_SPWT} = L_{m1} + L_{m2} + 2M \tag{3}$$

It should be noted that to ensure the same voltage gain characteristics as the conventional FB *LLC* converter, L_{m_SPWT} should be equal to the transformer magnetizing inductance of the conventional FB *LLC* converter. The operation principle of the proposed converter is the same as that of the conventional FB *LLC* converter.

The CM noise model of the proposed FB *LLC* converter has been developed to better illustrate the cancellation mechanism of CM noise displacement currents. First, the input and output dc capacitors are treated as a short circuit within the conducted EMI frequency range and LISN is characterized as a 25-Ω resistor [29]. Based on the two-capacitor transformer winding capacitance model [24], C_{AE} and C_{BE} (C_{CE} and C_{DE}) are used to model the lumped interwinding capacitors between the secondary windings and the primary winding *P*1 (*P*2), as shown in Fig. 4.

It should be pointed out that the interwinding capacitance between *P*1 and *P*2 does not introduce the CM noise current as the displacement current generated in that capacitance is confined within the transformer primary side. Then, the remaining circuit elements in Fig. 3 are replaced with CM noise sources by using substitution theory [30]. Q_1, Q_3, SR_1,

This article has been accepted for publication in IEEE Journal of Emerging and Selected Topics in Power Electronics. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2024.3386654

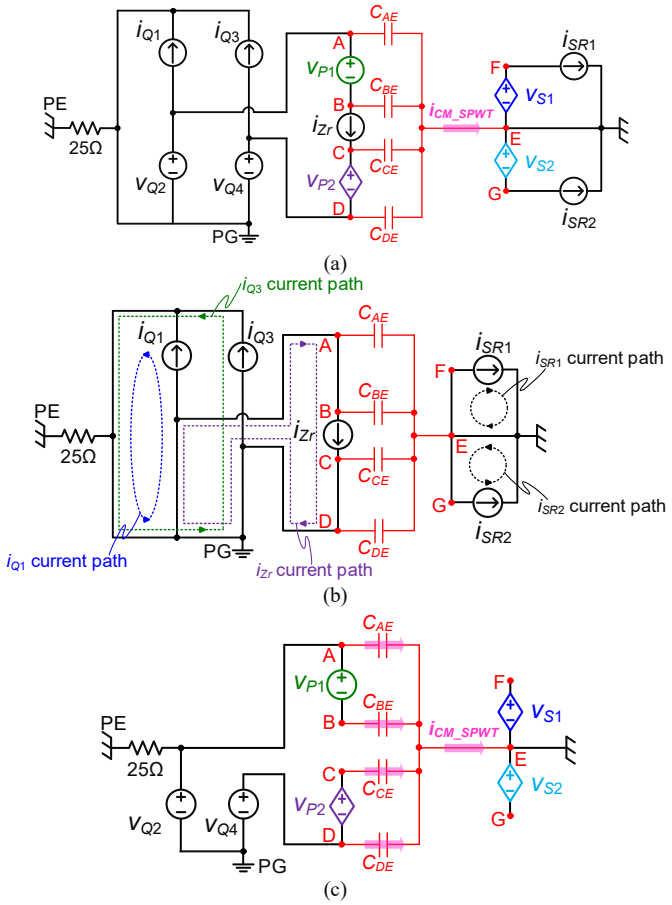


Fig. 5. CM noise equivalent circuits of proposed FB *LLC* resonant converter with SPWT configuration. (a) Equivalent CM noise coupling circuit by applying substitution theory. (b) Decoupled CM noise equivalent circuit with current noise sources. (c) Decoupled CM noise equivalent circuit with voltage noise sources.

SR_2, and resonant tank are substituted with current sources with their own current waveforms, which are denoted by i_{Q1}, i_{Q3}, i_{SR1}, i_{SR2}, and i_{Zr} respectively. Q_2, Q_4, and primary winding $P1$ are substituted with voltage sources with their own voltage waveforms, which are denoted by v_{Q2}, v_{Q4}, and v_{P1} respectively. Based on the transformer turns ratio, all other transformer windings are substituted with voltage-controlled voltage sources v_{P2}, v_{S1}, and v_{S2}. Since L_{m1} and L_{m2} are in parallel with voltage sources v_{P1} and v_{P2}, they are ignored in the CM noise analysis. Finally, the CM noise model of the proposed FB *LLC* converter is obtained, as shown in Fig. 5 (a).

In Fig. 5 (a), i_{CM_SPWT} represents the total CM noise displacement current flowing through the interwinding capacitance of the transformer. To calculate i_{CM_SPWT}, superposition theory is used to simplify the circuit. When analyzing one noise source, the other voltage sources are considered as short circuits and current sources are considered as open circuits. Fig. 5 (b) and (c) give the decoupled CM noise equivalent circuits with current and voltage noise sources, respectively. According to Fig. 5 (b), the current paths of i_{Q1}, i_{Q3}, and i_{Zr} are confined within the primary side. The current paths of i_{SR1} and i_{SR2} are confined within the secondary side. Hence, i_{Q1}, i_{Q3}, i_{SR1}, i_{SR2}, and i_{Zr} do not contribute to i_{CM_SPWT}, which are ignored. In Fig. 5 (c), v_{S1} and v_{S2} are open, which do not generate any CM noise currents. There are four remaining CM noise sources that are v_{Q2}, v_{Q4}, v_{P1}, and v_{P2}. Then, i_{CM_SPWT} can be calculated by (4). v_A, v_B, v_C, and v_D denote the electric potentials of transformer primary winding terminals with respect to PE, which are given in (5). As v_{Q2} and v_{Q4} are complementary (i.e., $v_{Q2} = -v_{Q4}$), it follows that v_A and v_D are also complementary (i.e., $v_A = -v_D$). Furthermore, since the split two primary windings have the same number of turns, by ignoring the leakage inductance, $v_{P1} = v_{P2}$. Thus, $v_B = v_{Q2} - v_{P1} = -v_{Q4} - v_{P2}$, which implies v_B and v_C are also complementary (i.e., $v_B = -v_C$). Based on this, (4) can be rewritten by (6). It is observed that i_{CM_SPWT} can be fully canceled if the transformer is made symmetrically, which means $C_{AE} = C_{DE}$ and $C_{BE} = C_{CE}$. As a result, the CM noise current generated in C_{AE} can be canceled by that generated in C_{DE}, and the CM noise current generated in C_{BE} can be canceled by that generated in C_{CE}, thereby resulting in a net CM noise current of zero.

$$i_{CM\_SPWT} = C_{AE}\frac{dv_A}{dt} + C_{DE}\frac{dv_D}{dt} + C_{BE}\frac{dv_B}{dt} + C_{CE}\frac{dv_C}{dt} \tag{4}$$

$$\begin{cases} v_A = v_{Q2} \\ v_B = v_{Q2} - v_{P1} \\ v_C = v_{Q4} + v_{P2} \\ v_D = v_{Q4} \end{cases} \tag{5}$$

$$i_{CM\_SPWT} = (C_{AE} - C_{DE})\frac{dv_A}{dt} + (C_{BE} - C_{CE})\frac{dv_B}{dt} \tag{6}$$

In some applications with fixed voltage gain requirements, the *LLC* resonant inductance is typically realized by utilizing the leakage inductance of the transformer. This, however, does not compromise the effectiveness of the proposed SPWT configuration in reducing CM noise. As shown in Fig. 5 (c), for winding $P1$ ($P2$), its leakage inductance is in series with the voltage source v_{P1} (v_{P2}). When the transformer is symmetrically wound, the leakage inductances of $P1$ and $P2$ can be considered equal. Consequently, the voltage drop caused by the leakage inductances of $P1$ and $P2$ is the same, as they carry identical resonant currents. As a result, v_B and v_C remain complementary, allowing CM noise currents in C_{BE} and C_{CE} to mutually cancel each other.

As discussed above, achieving a symmetrical winding arrangement is crucial for effectively reducing the CM noise displacement current generated in the transformer interwinding capacitance when utilizing the SPWT configuration. Specifically, the symmetrical condition refers to the equality of C_{AE} and C_{DE} as well as C_{BE} and C_{CE}.

The planar transformer structure is widely employed in *LLC* resonant converters due to its low height, low leakage inductance, high repeatability, and excellent thermal characteristics [31][32]. Compared to the wire-wound transformer, the planar transformer typically features a large interwinding capacitance between overlapping primary and secondary winding turns. Therefore, it is crucial to take this large parasitic interwinding capacitance into consideration to

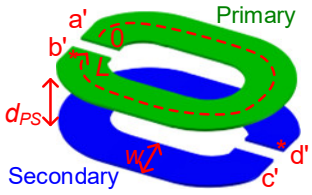


Fig. 6. 3D model of couple-turn when the layout is symmetrical.

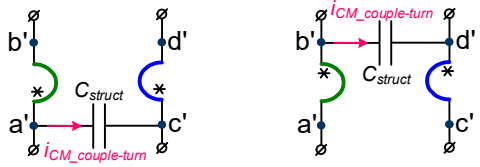


Fig. 7. Two types of one-capacitor models of couple-turn. (a) C_{struct} between corresponding terminals *a'* and *c'*. (b) C_{struct} between corresponding terminals *b'* and *d'*.

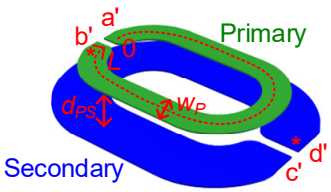


Fig. 8. 3D model of couple-turn when the layout is asymmetrical.

ensure the symmetrical winding arrangement for the planar transformer. However, the parasitic interwinding capacitance model of the transformer in Fig. 4 does not reflect the effects of parasitic capacitances between each winding turn, and thus cannot guide the symmetrical winding arrangement of the planar transformer. In the subsequent Section, the concept of couple-turn and its one-capacitor model will be reviewed, and an example analysis of symmetrical winding arrangement for the planar transformer will be presented. Finally, the concept of complementary couple-turns will be proposed to ensure the symmetrical winding arrangement for the planar transformer.

IV. Design of Symmetrical Planar Transformer for CM Noise Mitigation When Using SPWT Configuration

A. Review of Couple-Turn and Its One-Capacitor Model

Fig. 6 gives the 3D model of a couple-turn in the planar transformer [25]. Couple-turn denotes a pair of overlapping winding turns that belong to the primary and secondary winding respectively. It is assumed that the overlapping primary and secondary winding turns have a symmetrical layout. Hence, the parasitic structural interwinding capacitance C_{struct} of the couple-turn can be calculated by (7), where ε_0 denotes the permittivity of vacuum, $\varepsilon_{\text{Insul}}$ denotes the relative permittivity of the insulation material, d_{PS} denotes the distance between two winding turns, L and w denote the length and width of the winding turns.

$$C_{struct} = \varepsilon_0 \varepsilon_{\text{Insul}} \frac{w \cdot L}{d_{PS}} \tag{7}$$

According to the one-capacitor couple-turn model derived in [25], from the CM noise perspective, the parasitic structural interwinding capacitance of the couple-turn can be equivalently placed between a pair of corresponding terminals. There are two types of one-capacitor couple-turn models as shown in Fig. 7. Four terminals of the couple-turn are denoted by *a'*, *b'*, *c'*, and *d'*, which correspond to the terminal sequence letters in Fig. 6. Terminals *a'* and *c'* (*b'* and *d'*) on the couple-turn are a pair of corresponding terminals. $i_{CM\_couple\text{-}turn}$ denotes the CM noise current generated in the couple-turn. Either of the two types of models in Fig. 7 can be used to analyze and characterize the CM noise current in the couple-turn. The selection criterion aims to acquire a CM noise model of the planar transformer that enables straightforward analysis.

Asymmetric layouts of couple-turns are also common in the design of planar transformers. For example, when the secondary winding of the transformer has one turn per layer while the primary winding has multiple turns per layer, the couple-turns formed by the turns of the primary and secondary winding will inevitably have an asymmetric layout. It should be noted that in this case, the one-capacitor couple-turn model is still valid. When calculating the structural capacitance of the couple-turn, the non-overlapping area needs to be removed. Fig. 8 gives a typical example when the layout of the couple-turn is asymmetrical and C_{struct} can be recalculated as shown in (8), where w_P denotes the width of the primary winding turn. It is noted that the edge effect may introduce additional fringing capacitance [33]. (8) maintains its accuracy when most of the electric field energies are confined within the overlapping areas of the two winding turns.

$$C_{struct} = \varepsilon_0 \varepsilon_{\text{Insul}} \frac{w_P \cdot L}{d_{PS}} \tag{8}$$

B. Example Analysis of Symmetrical Winding Arrangement for Planar Transformer

A PCB-winding based planar transformer with a turns ratio of 8:2:2 is used here as an example to demonstrate the effectiveness of the proposed SPWT configuration. Two examples are analyzed which are both using the sandwich winding structure but different implementations of primary winding turns.

1) Example planar transformer #1*:* The sandwich winding arrangement and schematic of example planar transformer #1 are shown in Fig. 9 (a) and (b), respectively. The connections of winding terminals (*A*, *B*, *C*, *D*, *E*, *F*, and *G*) are shown in Fig. 3. This transformer includes two couple-turns: *P*1_4-*S*1_2 and *P*2_4-*S*2_2. Each turn in both the primary and secondary windings is implemented using a single layer. It is assumed that all turns have the same length and width, and the structural interwinding capacitances of the couple-turns *P*1_4-*S*1_2 and *P*2_4-*S*2_2 are considered equal by using the same insulation material with equal thickness, which are both denoted by C_{cell}.

Utilizing the one-capacitor couple-turn model, a lumped interwinding capacitance model of transformer #1 is shown in Fig. 9 (c). Here, v_B and v_{S1_2} (v_C and v_{S2_2}) denote the electric potentials of corresponding terminals for the couple-turn *P*1_4-*S*1_2 (*P*2_4-*S*2_2). The CM noise currents generated in couple-

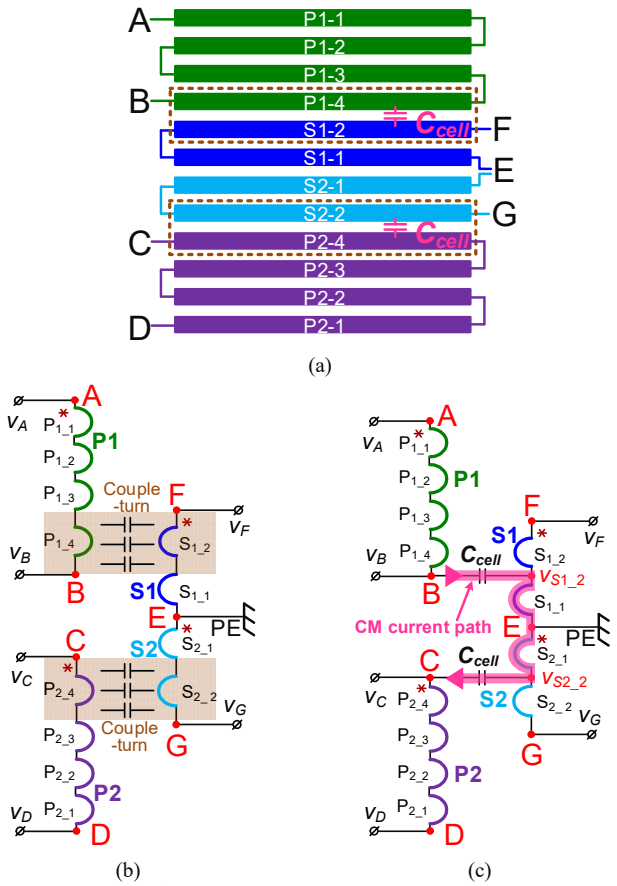


Fig. 9. Example planar transformer #1. (a) Transformer winding arrangement. (b) Transformer schematic. (c) CM noise current propagation path of transformer.

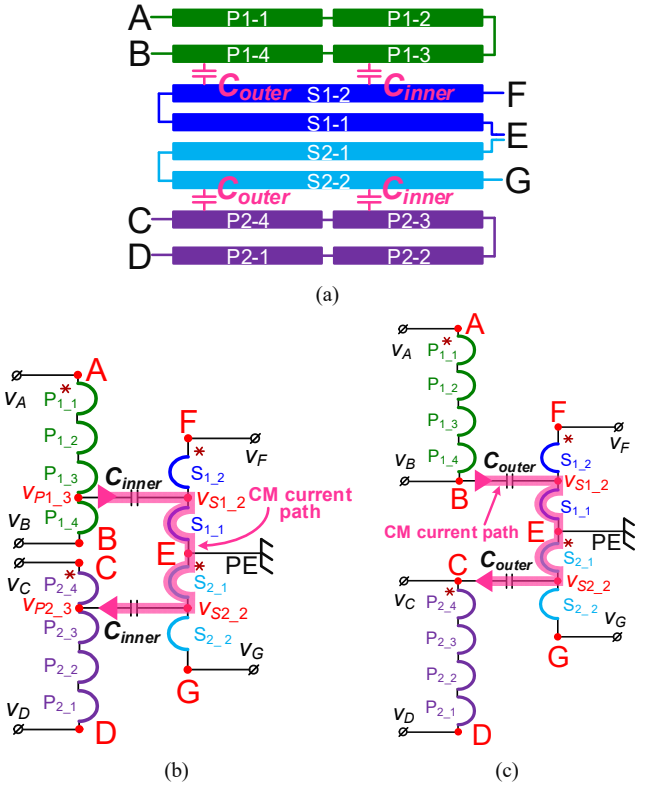


Fig. 10. Example planar transformer #2. (a) Transformer winding arrangement. (b) Propagation path of CM noise currents generated in couple-turns *P*1_3-*S*1_2 and *P*2_3-*S*2_2. (c) Propagation path of CM noise currents generated in couple-turns *P*1_4-*S*1_2 and *P*2_4-*S*2_2.

turns *P*1_4-*S*1_2 and *P*2_4-*S*2_2 are denoted by $i_{CM\#1\_P1\_4\text{-}S1\_2}$ and $i_{CM\#1\_P2\_4\text{-}S2\_2}$, which can be calculated using (9) and (10), respectively.

$$i_{CM\#1\_P1\_4\text{-}S1\_2} = C_{cell}\frac{d(v_B - v_{S1\_2})}{dt} \tag{9}$$

$$i_{CM\#1\_P2\_4\text{-}S2\_2} = C_{cell}\frac{d(v_C - v_{S2\_2})}{dt} \tag{10}$$

As the value of the winding turn resistance is significantly smaller than that of the inductance, the voltage difference between any two adjacent winding turns can be considered as constant. Consequently, v_{S1_2} and v_{S2_2} are calculated as $v_F/2$ and $v_G/2$ which are complementary (i.e., v_{S1_2} = -v_{S2_2}), and similarly, v_B and v_C are also complementary (i.e., v_B = -v_C). As a result, $i_{CM\#1\_P1\_4\text{-}S1\_2}$ = -$i_{CM\#1\_P2\_4\text{-}S2\_2}$, indicating the CM noise current generated in couple-turn *P*1_4-*S*1_2 can be completely canceled by the CM noise current generated in couple-turn *P*2_4-*S*2_2. The CM current path shown in Fig. 9 (c) illustrates that there is no additional CM current coupling into the secondary side, leading to a net CM noise current of zero. In conclusion, transformer #1 is symmetrical from the CM noise perspective.

2) Example planar transformer #2: Fig. 10 (a) illustrates the winding arrangement of example planar transformer #2. Different from transformer #1, the primary winding turns are implemented with two turns per layer. There are four couple-turns which are *P*1_4-*S*1_2, *P*1_3-*S*1_2, *P*2_4-*S*2_2, and *P*2_3-*S*2_2. It is noted that couple-turns *P*1_4-*S*1_2 and *P*2_4-*S*2_2 have the same structural interwinding capacitance since they have the same overlapping area and the same isolation material with equal thickness. The conclusion is the same for the couple-turns *P*1_3-*S*1_2 and *P*2_3-*S*2_2. The structural interwinding capacitances of couple-turns *P*1_4-*S*1_2 and *P*2_4-*S*2_2 (*P*1_3-*S*1_2 and *P*2_3-*S*2_2) are denoted by C_{outer} (C_{inner}).

Fig. 10 (b) gives the selected one-capacitor models of couple-turns *P*1_3-*S*1_2 and *P*2_3-*S*2_2. v_{P1_3} and v_{S1_2} (v_{P2_3} and v_{S2_2}) are the electric potentials of corresponding terminals for the couple-turn *P*1_3-*S*1_2 (*P*2_3-*S*2_2). The CM noise currents generated in these two couple-turns are denoted by $i_{CM\#2\_P1\_3\text{-}S1\_2}$ and $i_{CM\#2\_P2\_3\text{-}S2\_2}$, which can be calculated as shown in (11) and (12), respectively.

$$i_{CM\#2\_P1\_3\text{-}S1\_2} = C_{inner}\frac{d(v_{P1\_3} - v_{S1\_2})}{dt} \tag{11}$$

$$i_{CM\#2\_P2\_3\text{-}S2\_2} = C_{inner}\frac{d(v_{P2\_3} - v_{S2\_2})}{dt} \tag{12}$$

Assuming a constant voltage difference between any two adjacent primary winding turns, v_{P1_3} and v_{P2_3} are calculated as shown in (13). As a result of the complementary electric potentials of v_A and v_D, v_B and v_C, the potentials of v_{P1_3} and v_{P2_3} are complementary (i.e., v_{P1_3} = -v_{P2_3}). Additionally,

since v_{S1_2} and v_{S2_2} are complementary as well (i.e., v_{S1_2} = -v_{S2_2}), $i_{CM\#2\_P1\_3\text{-}S1\_2}$ and $i_{CM\#2\_P2\_3\text{-}S2\_2}$ can be completely canceled by each other.

$$\begin{cases} v_{P1-3}=v_A-3\dfrac{(v_A-v_B)}{4}=\dfrac{v_A}{4}+\dfrac{3v_B}{4} \\ v_{P2-3}=v_D+3\dfrac{(v_C-v_D)}{4}=\dfrac{v_D}{4}+\dfrac{3v_C}{4} \end{cases} \tag{13}$$

Fig. 10 (c) gives the selected one-capacitor models of couple-turns *P*1_4-*S*1_2 and *P*2_4-*S*2_2. v_B and v_{S1_2} (v_C and v_{S2_2}) are the electric potentials of corresponding terminals for the couple-turn *P*1_4-*S*1_2 (*P*2_4-*S*2_2). The CM noise currents generated in these two couple-turns are denoted by $i_{CM\#2\_P1\_4\text{-}S1\_2}$ and $i_{CM\#2\_P2\_4\text{-}S2\_2}$, which can be calculated as shown in (14) and (15), respectively. Owing to the complementary electric potentials of v_B and v_C, v_{S1_2} and v_{S2_2}, $i_{CM\#2\_P1\_4\text{-}S1\_2}$ and $i_{CM\#2\_P2\_4\text{-}S2\_2}$ can be completely canceled by each other. Therefore, the total CM noise displacement current generated in transformer #2 is zero, which indicates that transformer #2 is symmetrical from the CM noise perspective.

$$i_{CM\#2\_P1\_4\text{–}S1\_2}=C_{outer}\frac{d(v_B-v_{S1\_2})}{dt} \tag{14}$$

$$i_{CM\#2\_P2\_4\text{–}S2\_2}=C_{outer}\frac{d(v_C-v_{S2\_2})}{dt} \tag{15}$$

C. Concept of Complementary Couple-Turns

The concept of complementary couple-turns is proposed in this part. Complementary couple-turns refer to a pair of couple-turns that generate complementary CM noise currents, which can be completely canceled by each other. For instance, in example planar transformer #1, *P*1_4-*S*1_2 and *P*2_4-*S*2_2 are a pair of complementary couple-turns. Similarly, as shown in example planar transformer #2, *P*1_4-*S*1_2 and *P*2_4-*S*2_2 (*P*1_3-*S*1_2 and *P*2_3-*S*2_2) are also a pair of complementary couple-turns.

In SPWT configuration based center-tapped planar transformer, there are two types of complementary couple-turns, as shown in Fig. 11 (a) and (b). Fig. 11 (a) shows the complementary couple-turns *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n*. Fig. 11 (b) shows the complementary couple-turns *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n*. *P*1_*m* (*P*2_*m*) is defined as the *m*th primary winding turn of *P*1 (*P*2) from terminal *A* (*D*). *S*1_*n* (*S*2_*n*) is defined as the *n*th secondary winding turn of *S*1 (*S*2) from terminal *E*. N_s denotes the turns number of secondary windings *S*1 and *S*2. N_{P1} and N_{P2} denote the turns number of primary windings *P*1 and *P*2, respectively.

In Fig. 11, the corresponding terminals of all complementary couple-turns are denoted by black dots. It should be noted that the difference between couple-turn *P*1_*m*-*S*1_*n* in Fig. 11 (a) and couple-turn *P*1_*m*-*S*2_*n* in Fig. 11 (b) lies in the distribution of their corresponding terminals. Specifically, in *P*1_*m*-*S*1_*n*, the corresponding terminals of the primary and secondary winding turns are oriented in the same direction, while in *P*1_*m*-*S*2_*n* they are oriented in opposite directions. In other words, the *dv*/*dt* phase of the primary and secondary winding turns are the same in *P*1_*m*-*S*1_*n*, but opposite in *P*1_*m*-*S*2_*n*. As a result, there will be different CM noise behaviors for the couple-turns *P*1_*m*-*S*1_*n* and *P*1_*m*-*S*2_*n*, which is the fundamental reason for the existence of two types of complementary couple-turns.

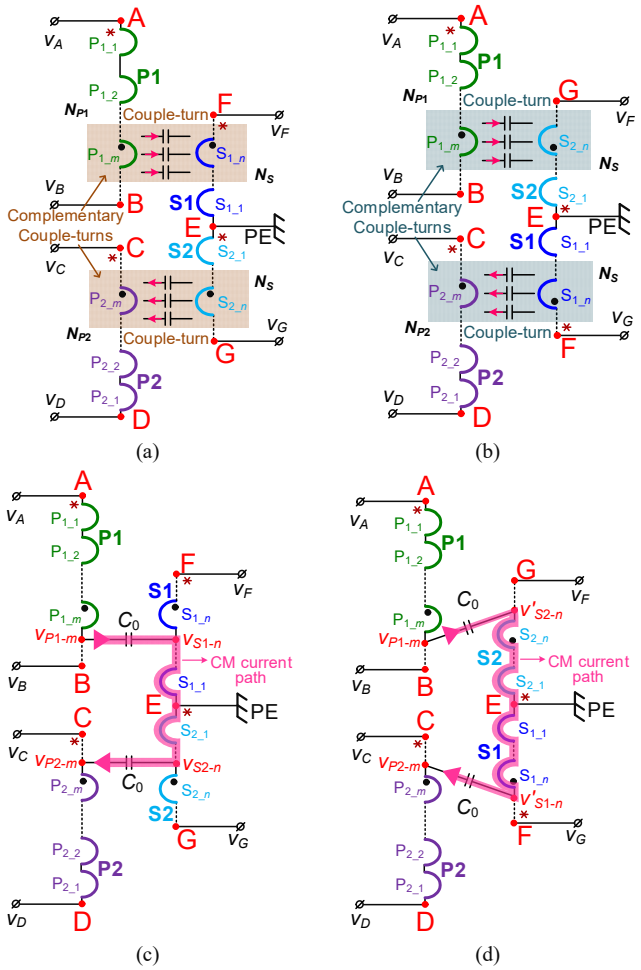


Fig. 11. Two types of complementary couple-turns. (a) Complementary couple-turns *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n*. (b) Complementary couple-turns *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n*. (c) Propagation path of CM noise currents generated in *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n*. (d) Propagation path of CM noise currents generated in *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n*.

Based on the one-capacitor couple-turn model, Fig. 11 (c) and (d) give the lumped interwinding capacitance model of couple-turns shown in Fig. 11 (a) and (b), respectively. In Fig. 11 (c), v_{P1_m} and v_{S1_n} (v_{P2_m} and v_{S2_n}) denote the electric potentials of corresponding terminals for the couple-turn *P*1_*m*-*S*1_*n* (*P*2_*m*-*S*2_*n*). In Fig. 11 (d), v_{P1_m} and v'_{S2_n} (v_{P2_m} and v'_{S1_n}) denote the electric potentials of corresponding terminals for the couple-turn *P*1_*m*-*S*2_*n* (*P*2_*m*-*S*1_*n*). By ignoring the impact of the leakage inductance and assuming a unit coupling coefficient, the voltage difference between any two adjacent winding turns is considered as a constant value, denoted as Δv, which can be calculated by (16). v_{P1_m}, v_{P2_m}, v_{S1_n}, v_{S2_n}, v'_{S1_n}, and v'_{S2_n} are calculated accordingly as shown in (17)-(22). The CM noise currents generated in couple-turns *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n* are denoted by $i_{CM\_P1\_m\text{-}S1\_n}$ and $i_{CM\_P2\_m\text{-}S2\_n}$, which can be calculated as shown in (23) and (24), by assuming a constant parasitic structural interwinding capacitance C_0 of each couple-turn. Based on (23) and (24), since v_A = -v_D, it can be concluded that $i_{CM\_P1\_m\text{-}S1\_n}$ =

$-i_{CM\_P2\_m\text{-}S2\_n}$, implying that couple-turns *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n* have complementary CM noise displacement currents that can be canceled by each other. Hence, *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n* are a pair of complementary couple-turns.

$$\Delta v=\frac{v_A-v_B}{N_{P1}}=\frac{v_C-v_D}{N_{P2}}=\frac{v_F-v_E}{N_S}=\frac{v_E-v_G}{N_S} \tag{16}$$

$$v_{P1\_m}=v_A-m\Delta v \tag{17}$$

$$v_{P2\_m}=v_D+m\Delta v \tag{18}$$

$$v_{S1\_n}=(n-1)\Delta v \tag{19}$$

$$v_{S2\_n}=-(n-1)\Delta v \tag{20}$$

$$v'_{S1\_n}=n\Delta v \tag{21}$$

$$v'_{S2\_n}=-n\Delta v \tag{22}$$

$$i_{CM\_P1\_m\text{–}S1\_n}=C_0\frac{d(v_{P1\_m}-v_{S1\_n})}{dt}=C_0\frac{d(v_A-(m+n-1)\Delta v)}{dt} \tag{23}$$

$$i_{CM\_P2\_m\text{–}S2\_n}=C_0\frac{d(v_{P2\_m}-v_{S2\_n})}{dt}=C_0\frac{d(v_D+(m+n-1)\Delta v)}{dt} \tag{24}$$

Likewise, based on Fig. 11 (d), the CM noise displacement currents generated in couple-turns *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n* are given in (25) and (26). Since $v_A = -v_D$, it can be concluded that $i_{CM\_P1\_m\text{-}S2\_n} = -i_{CM\_P2\_m\text{-}S1\_n}$, implying that *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n* are also a pair of complementary couple-turns.

$$i_{CM\_P1\_m\text{–}S2\_n}=C_0\frac{d(v_{P1\_m}-v'_{S2\_n})}{dt}=C_0\frac{d(v_A-(m-n)\Delta v)}{dt} \tag{25}$$

$$i_{CM\_P2\_m\text{–}S1\_n}=C_0\frac{d(v_{P2\_m}-v'_{S1\_n})}{dt}=C_0\frac{d(v_D+(m-n)\Delta v)}{dt} \tag{26}$$

The use of complementary couple-turns enables the effective reduction of CM noise in planar transformers. The cancellation of CM noise is achieved by designing the winding arrangement and interwinding capacitance in such a way that the CM noise currents generated in the complementary couple-turns are equal in magnitude and opposite in phase.

D. Symmetrical Winding Arrangement Based on Complementary Couple-Turns

Based on the previous analysis, the planar transformer winding arrangement can be symmetrical from the CM noise perspective and the total CM noise displacement current generated in the planar transformer can be fully canceled when the following two conditions are satisfied:

1) Overlapping layers should be selected based on the concept of complementary couple-turns. There are two types of complementary couple-turns: *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n*, as well as *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n*. Definitions for *P*1_*m*-*S*1_*n*, *P*2_*m*-*S*2_*n*, *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n* are provided in Fig. 11.

If the *m*th winding turn of *P*1 is overlapped with the *n*th winding turn of *S*1, the *m*th winding turn of *P*2 needs to be overlapped with the *n*th winding turn of *S*2 so as to generate the complementary CM noise current. Likewise, If the *m*th winding turn of *P*1 is overlapped with the *n*th winding turn of *S*2, the *m*th winding turn of *P*2 needs to be overlapped with the *n*th winding turn of *S*1.

2) The complementary couple-turns should be designed to have the same parasitic structural interwinding capacitances.

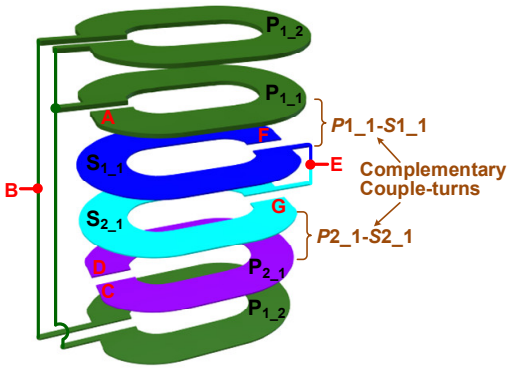


Fig. 12. Transformer winding arrangement of example planar transformer #3.

This is typically achieved through the symmetrical layout of complementary couple-turns. It should be noted that the thicknesses of insulation layers in most multi-layer PCBs are not consistent. When constructing planar transformers using a single PCB board, attention should be given to the interlayer FR4 distance to ensure the same parasitic structural interwinding capacitances of complementary couple-turns.

Complementary couple-turns offer the advantage of utilizing the inherent coupling capacitance between the primary and secondary sides of a planar transformer to cancel out CM currents generated within the transformer. This eliminates the need for additional shielding layers or extra transformer windings. Furthermore, the utilization of complementary couple-turns is entirely compatible with the interleaved winding structure. This compatibility arises from the fact that the overlapping layers introduced by the interleaved winding structure can be harnessed to create complementary couple-turns. Consequently, the trade-off between the interleaved winding structure and the CM noise performance of the transformer is eliminated. Unlike the conventional winding methods for planar transformers mentioned in [15]-[17], the overlapping primary and secondary winding layers of the transformer do not need to have identical voltage distributions. This significantly enhances the designer's flexibility when creating the structure of planar transformers. It should be pointed out that the concept of complementary couple-turns cannot be used to reduce the CM noise for the phase-shift control based FB *LLC* resonant converter. With the phase-shift control, the electric potentials of two phase-leg midpoints change at different times, and the generated CM noise displacement currents flowing through the associated parasitic capacitance cannot be mutually canceled.

Even if the number of turns in the primary winding is odd, the proposed complementary couple-turns can still be utilized to ensure a symmetrical transformer winding arrangement when using the SPWT configuration. A planar transformer with a turns ratio of 3:1:1 is used as an example. Fig. 12 illustrates the winding arrangement of example planar transformer #3. The connections of winding terminals (*A*, *B*, *C*, *D*, *E*, *F*, and *G*) are shown in Fig. 3. In this figure, *P*1_1-*S*1_1 and *P*2_1-*S*2_1 represent a complementary pair of couple-turns. Based on (23) and (24), the CM noise currents generated

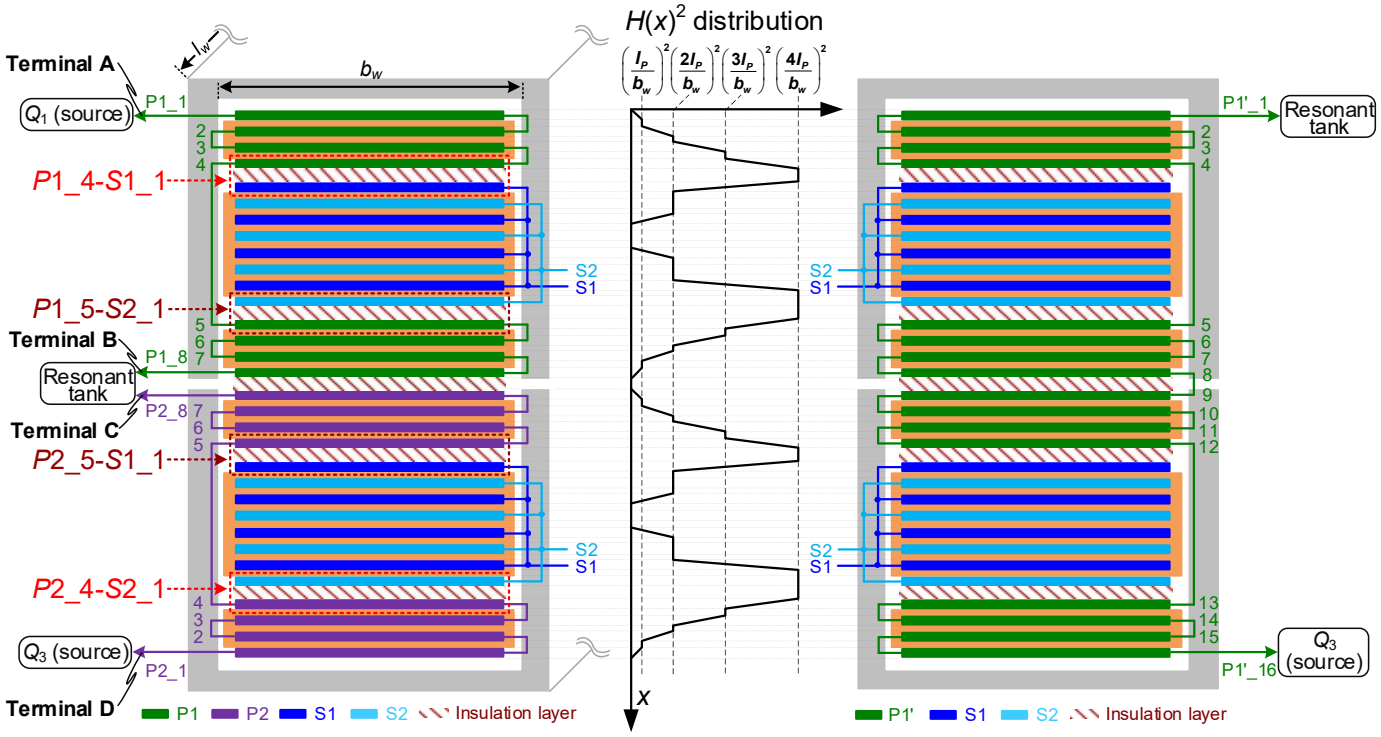


Fig. 13. (a) Transformer winding arrangement and terminal connections of proposed FB *LLC* resonant converter. Refer to Fig. 3 for locations of Q_1 (source), Q_3 (source), and resonant tank. (b) Distribution of $H(x)^2$ for both proposed and conventional planar transformers. (c) Transformer winding arrangement and terminal connections of conventional FB *LLC* resonant converter. Refer to Fig. 1 for locations of Q_3 (source) and resonant tank.

in these two couple-turns can be calculated as shown in (27) and (28), respectively. The parasitic structural capacitances of *P*1_1-*S*1_1 and *P*2_1-*S*2_1 are denoted by $C_{P1\_1\text{-}S1\_1}$ and $C_{P2\_1\text{-}S2\_1}$, which are considered equal by using the same insulation material with equal thickness. Since v_A and v_D are complementary (i.e., $v_A = -v_D$), it follows that $i_{CM\#3\_P1\_1\text{-}S1\_1}$ and $i_{CM\#3\_P2\_1\text{-}S2\_1}$ are also complementary. In conclusion, the CM noise currents generated in these two couple-turns can mutually cancel each other.

$$i_{CM\#3\_P1\_1\text{–}S1\_1} = C_{P1\_1\text{–}S1\_1}\frac{d(v_A - \Delta v)}{dt} \tag{27}$$

$$i_{CM\#3\_P2\_1\text{–}S2\_1} = C_{P2\_1\text{–}S2\_1}\frac{d(v_D + \Delta v)}{dt} \tag{28}$$

*P*1_2 in transformer #3 is split into two parallel winding turns that are placed on the top and bottom layers, respectively. *P*1_2 does not overlap with the turns of the secondary winding. As a result, *P*1_2 does not generate any additional CM noise current, and transformer #3 remains symmetrical from the CM noise perspective.

In general, when the number of turns in the original primary winding of a planar transformer is odd, it is not possible to have an equal number of turns in both *P*1 and *P*2. Specifically, if the number of turns in *P*1 is one more than that of *P*2 (i.e., $N_{P1} = N_{P2} + 1$), an additional CM noise displacement current will be induced by the primary winding turn *P*1_N_{P1} if it overlaps with the secondary winding turns. To avoid this issue, it is necessary to ensure that *P*1_N_{P1} does not overlap with the secondary winding turns.

V. Practical Considerations

This section discusses the influences of SPWT configuration on the FB *LLC* converter, including transformer leakage inductance, transformer winding loss, and voltage conversion ratio.

In Fig. 13 (a) and (c), two center-tapped planar transformers with a turns ratio of 16:1:1 are presented. Fig. 13 (a) corresponds to the transformer designed for the proposed Split Primary Winding FB *LLC* converter as shown in Fig. 3, while Fig. 13 (c) corresponds to the transformer designed for the conventional FB *LLC* converter as shown in Fig. 1. For a fair comparison, apart from the different terminal connections of the primary windings, the construction methods for these two transformers are identical. It should be pointed out that the proposed planar transformer can be rendered identical to the conventional planar transformer by short-circuiting terminals *B* and *C*, and subsequently connecting the resonant tank to terminal *A*. As shown in Fig. 13 (c), for the conventional planar transformer, there is only one primary winding which is denoted by *P*1'. *P*1'_1 is the first primary winding turn which is connected to the resonant tank. *P*1'_16 is the last primary winding turn which is connected to Q_3 (Source) in Fig. 1. As shown in Fig. 13 (a), for the proposed planar transformer, there are two primary windings which are *P*1 and *P*2. *P*1_1 is the first primary winding turn of *P*1, which is connected to Q_1 (Source) in Fig. 3. *P*2_1 is the first primary winding turn of *P*2, which is connected to Q_3 (Source) in Fig. 3. The resonant tank

is connected between *P*1_8 and *P*2_8, which are the last primary winding turns of *P*1 and *P*2, respectively. The remaining specifications for these two transformers are identical and can be summarized as follows:

1) DMR96 ferrite core material from DMEGC is selected and the core size is ECW34C (customized from DMEGC). The specific structure and dimensions of ECW34C are provided in Fig. 14. There is an approximately 0.22 mm air gap in the middle of the center column and the two side columns of the magnetic core. Three air gaps are all filled with Kapton tapes.

2) The transformer windings are designed with a single turn per layer, each having the same width of 8 mm. Instead of the sandwich winding structure shown in Fig. 9 (a) and Fig. 10 (a), a partial interleaved winding structure is employed by stacking six PCBs. The choice of a partial interleaved winding structure in the final design aims to achieve lower ac losses for the transformer windings, which means higher system efficiency. Specifically, the primary windings are constructed by using four 4-layer 4 OZ PCBs with a PCB board thickness of 1.63 mm, while the secondary windings are constructed by using two 8-layer 4 OZ PCBs with a PCB board thickness of 2.41 mm. Detailed layer stack-up structures of the primary and secondary winding PCBs are provided in Table I and Table II, respectively. The insulation layers between different PCBs are implemented by 0.25 mm electrical insulation papers with a relative permittivity of 2.6 [34].

For the proposed planar transformer, there are two pairs of complementary couple-turns which are *P*1_4-*S*1_1 and *P*2_4-*S*2_1, *P*1_5-*S*2_1 and *P*2_5-*S*1_1. Since 6 PCBs are stacked by using the same type of insulation material with the same thickness, the complementary couple-turns have the same parasitic structural interwinding capacitances. Thus, this planar transformer is symmetrical from the CM noise perspective and the total CM noise displacement current should be significantly reduced.

A. Transformer Leakage Inductance and Winding Loss

The leakage inductance referred to the primary side can be calculated by (29), demonstrating that the energy stored in the leakage inductance equals the leakage magnetic field energy. By calculating the total energy of the leakage magnetic field, the theoretical value of the leakage inductance can be determined. Here, the total energy of the leakage magnetic field refers to the summation of energies stored in the primary winding layers, secondary winding layers, and insulation layers.

$$E_{energy} = \frac{\mu_0}{2} \int_{\substack{window \\ area}} H^2 dV = \frac{1}{2} L_{lk} I_P^2 \tag{29}$$

where L_{lk} is the leakage inductance in the primary side, I_P is the current of the primary winding, and H is the magnetic field intensity in the window.

For the proposed planar transformer, because the primary windings *P*1 and *P*2 are connected in series, the currents in these windings are equal and denoted as I_P. Assuming the magnetic field intensity is constant in the horizontal direction, the leakage inductance can be calculated as

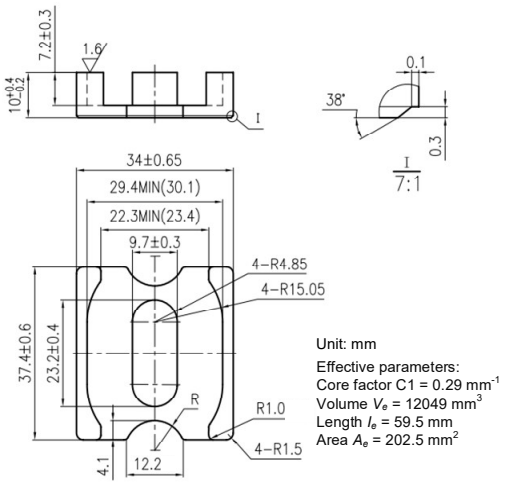


Fig. 14. Specific structure and dimensions of ECW34C magnetic core.

TABLE I
STACK-UP STRUCTURE OF PRIMARY WINDING PCBS

Layer	Stack up	Thickness (mm)
	Solder Mask	0.02
L1	3 OZ+ Plating	0.14
	Prepreg (FR4)	0.28
L2	4 OZ	0.14
	Core (FR4)	0.47
L3	4 OZ	0.14
	Prepreg (FR4)	0.28
L4	3 OZ + Plating	0.14
	Solder Mask	0.02

TABLE II
STACK-UP STRUCTURE OF SECONDARY WINDING PCBS

Layer	Stack up	Thickness (mm)
	Solder Mask	0.025
L1	3 OZ + Plating	0.14
	Prepreg (FR4)	0.16
L2	4 OZ	0.14
	Prepreg (FR4)	0.12
L3	4 OZ	0.14
	Prepreg (FR4)	0.28
L4	4 OZ	0.14
	Core (FR4)	0.12
L5	4 OZ	0.14
	Prepreg (FR4)	0.28
L6	4 OZ	0.14
	Prepreg (FR4)	0.12
L7	4 OZ	0.14
	Prepreg (FR4)	0.16
L8	3 OZ + Plating	0.14
	Solder Mask	0.025

$$L_{lk} = \frac{\mu_0}{I_P^2} \int_V H(x)^2 dx = \frac{\mu_0 b_w l_w}{I_P^2} \int_0^x H(x)^2 dx \tag{30}$$

where V is the total volume of window area, b_w is the width of the magnetic core window, l_w is the depth of the magnetic core, $H(x)$ is the magnetic field intensity in the direction the geometric position x (see Fig. 13 (b)). Based on (30), the leakage inductance is proportional to the integral of the square of the magnetic field intensity. Hence, the distribution of $H(x)^2$

provides an intuitive reflection of the magnitude of the leakage inductance. The graphical interpretation of the $H(x)^2$ distribution is depicted in Fig. 13 (b), in accordance with Ampere's circuital theorem. It is noted that secondary windings $S1$ and $S2$ conduct alternately for half of the switching period, and Fig. 13 (b) is based on the operating scenario where $S1$ conducts. Due to the identical winding arrangement in both the proposed and conventional planar transformers, they exhibit the same $H(x)^2$ distribution. In other words, their leakage inductance performance is the same. The same conclusion can be drawn when analyzing the operating scenario where $S2$ conducts.

It should be pointed out that the previous discussion does not take into account the effects of eddy current when the transformer operates under high-frequency (HF) conditions. In HF range, both the skin effect and proximity effect cause the winding current to concentrate near the conductor's surface. This phenomenon leads to an inhomogeneous distribution of $H(x)^2$, consequently changing the total leakage magnetic field energy.

On the other hand, the skin effect and proximity effect also contribute to increased ac resistance of the transformer windings, which can be explained by Ferreira's formula [35]:

$$R_{tx\_ac} = R_{tx\_dc} \cdot (F_{skin} + F_{proximity}) \tag{31}$$

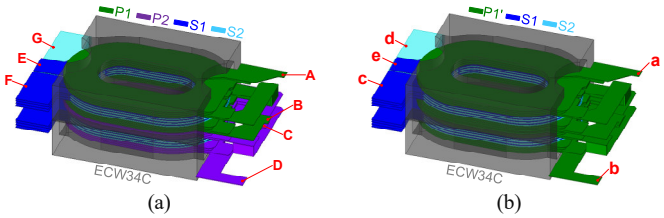
where F_{skin} and $F_{proximity}$ represent the skin effect ratio and proximity effect ratio, respectively. Their expressions are given by

$$F_{skin} = \frac{\xi}{2} \cdot \frac{\sinh(\xi) + \sin(\xi)}{\cosh(\xi) - \cos(\xi)}, \quad \xi = \frac{h}{\delta} \tag{32}$$

$$F_{proximity} = \frac{\xi}{2} \cdot \left(\frac{2F(h)}{F(h) - F(0)} - 1\right)^2 \cdot \left(\frac{\sinh(\xi) - \sin(\xi)}{\cosh(\xi) + \cos(\xi)}\right) \tag{33}$$

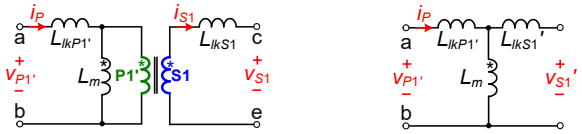
where h denotes the thickness of conductors, and δ stands for the skin depth at the operating frequency. $F(h)$ and $F(0)$ correspond to the magnetomotive forces (MMFs) at the borders of the conductor, which depend on the transformer's winding arrangement. To mitigate the influence of the skin effect, the general design criterion is to ensure that the conductor thickness remains less than twice the skin depth. To mitigate the influence of the proximity effect, an interleaved structure is commonly employed in planar transformer applications. This structure reduces the MMF that drives lower $F_{proximity}$. Both the proposed and conventional planar transformers have equal conductor thickness for their primary and secondary windings, resulting in the same F_{skin} value under the same operating frequency. Furthermore, their winding arrangements are identical, theoretically yielding the same MMF distribution and the same $F_{proximity}$ value under the same operating frequency. Consequently, these two transformers have equal additional losses introduced by the skin and proximity effects.

To quantitatively analyze the leakage inductance and winding loss, a 3D Finite Element Analysis (FEA) simulation is conducted using Maxwell software. Fig. 15 presents 3D models of the proposed and conventional transformers. The interlayer distances of transformer winding turns are selected based on Tables I and II. To save simulation time, PCB vias are removed and the rounded corners of the magnetic core are replaced by right angles. The Maxwell solver is eddy current type and the excitation is 150 kHz current. As mentioned earlier, secondary windings $S1$ and $S2$ conduct alternately during half of the switching period. Therefore, each simulation model in Fig. 15 is executed twice to determine the transformer's leakage inductance and ac/dc resistance ratio.



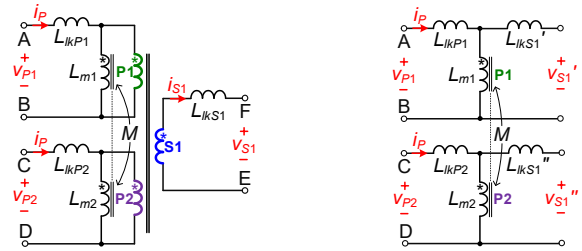
(a) (b)

Fig. 15. Maxwell 3D models of (a) proposed and (b) conventional transformers.



(a) (b)

Fig. 16. (a) π model of conventional transformer. (b) Equivalent model used for calculating total leakage inductance.



(a) (b)

Fig. 17. (a) π model of proposed transformer. (b) Equivalent model used for calculating total leakage inductance.

1) Simulation of leakage inductance: Fig. 16 (a) presents the π model of the conventional transformer, corresponding to the operating scenario where $S1$ conducts. $L_{lkP1'}$ and L_{lkS1} denote the leakage inductances for the primary winding $P1'$ and secondary winding $S1$, respectively. The total leakage inductance referred to the primary side is denoted by $L_{lkP\_S1\_conv}$, which can be measured from the primary winding terminals when the secondary winding $S1$ is short-circuited. Notably, $L_{lkP\_S1\_conv}$ includes both the primary leakage inductance $L_{lkP1'}$ and secondary reflected leakage inductance. When $S1$ is short-circuited, the secondary leakage inductance L_{lkS1} is reflected to the primary side, resulting in L_{lkS1}', as illustrated in Fig. 16 (b). Consequently, $L_{lkP\_S1\_conv}$ is approximated as $L_{lkP1'} + L_{lkS1}'$.

Fig. 17 (a) presents the π model of the proposed transformer, corresponding to the operating scenario where $S1$ conducts. L_{lkP1} and L_{lkP2} denote the leakage inductances for the primary windings. The total leakage inductance referred to the primary side is denoted by $L_{lkP\_S1\_prop}$, which can also be measured from the primary winding terminals when the secondary winding $S1$ is short-circuited. Notably, $L_{lkP\_S1\_prop}$ includes both the primary leakage inductances and secondary reflected leakage inductances. When $S1$ is short-circuited, the

TABLE III
SIMULATED LEAKAGE INDUCTANCES (UNIT: μH)

Conventional	$L_{lkP\_S1\_conv}$	1.14
	$L_{lkP\_S2\_conv}$	1.13
Proposed	$L_{lkP\_S1\_prop}$	1.14
	$L_{lkP\_S2\_prop}$	1.13

TABLE IV
SIMULATED AC/DC RESISTANCE RATIOS AT 150 KHZ

	Conventional	Proposed
Primary winding(s)	1.78	1.78
Secondary winding $S1$	2.141	2.139
Secondary winding $S2$	2.096	2.1

secondary leakage inductance L_{lkS1} is reflected to the primary side, resulting in L_{lkS}' and L_{lkS}'', as illustrated in Fig. 17 (b). Consequently, $L_{lkP\_S1\_prop}$ is approximated as L_{lkP1} + L_{lkP2} + L_{lkS}'+ L_{lkS}''.

The simulated total leakage inductances for the conventional and proposed transformers are provided in Table III. It can be observed that, whether $S1$ is conducting or $S2$ is conducting, the conventional and proposed planar transformers exhibit the same total leakage inductance.

2) Simulation of ac/dc resistance ratio: As shown in (31), the ac/dc resistance ratio refers to the summation of F_{skin} and $F_{proximity}$, which determines transformer winding losses. The benchmark for calculating the ac/dc resistance ratio is established through a 60-Hz simulation, during which the skin and proximity effects are negligible. A comparison of solid losses between simulation results at 150 kHz and 60 Hz enables a convenient determination of the ac/dc resistance ratio. The 3D FEA simulation results are presented in Table IV. It is observed that the conventional and proposed planar transformers exhibit similar ac/dc resistance ratios for both primary and secondary windings.

In summary, the SPWT configuration based planar transformer, when compared to the conventional planar transformer, demonstrates similar performance in terms of leakage inductance and winding loss. This similarity arises from the fact that the two primary windings in the proposed planar transformer are connected in series, ensuring identical conduction currents in both primary windings. By utilizing the same construction approach as the conventional planar transformer, the proposed transformer presents the equivalent leakage magnetic field energy and eddy current effects.

B. Voltage Conversion Ratio

The voltage regulation of *LLC* converters can be affected by interwinding capacitances when employing the SPWT configuration. As shown in Fig. 18, these capacitances include not only those between the primary and secondary windings but also capacitances between the primary windings $P1$ and $P2$. Here, C_{AD} and C_{BC} are used to model the interwinding capacitors between $P1$ and $P2$. It can be observed that C_{BC}, C_{BE} and C_{CE} will participate in the resonance of L_r and C_r, potentially affecting the gain performance of the FB *LLC* converter under HF operation conditions.

The impedance of the resonant unit consisting of L_r, C_r, C_{BC},

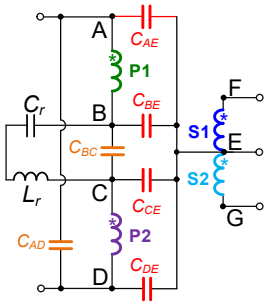


Fig. 18. Complete interwinding capacitance model of SPWT configuration based planar transformer.

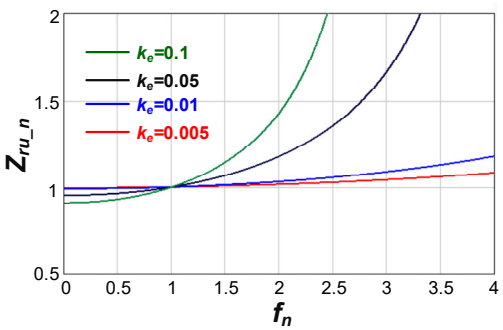


Fig. 19. Variation of Z_{ru_n} concerning frequency changes.

C_{BE}, and C_{CE} is calculated as

$$Z_{ru}(s) = \frac{C_r L_r s^2 + 1}{s(C_r C_e L_r s^2 + C_r + C_e)} \tag{34}$$

where

$$s = j\omega_s, \quad \omega_s = 2\pi f_s, \quad C_e = C_{BC} + \frac{C_{BE} C_{CE}}{C_{BE} + C_{CE}} \tag{35}$$

C_e represents the equivalent capacitance in parallel with the resonant tank. The impedance zero and pole of Z_{ru} are given by (36) and (37), respectively.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{36}$$

$$f_p = \frac{1}{2\pi\sqrt{L_r \dfrac{C_r C_e}{C_r + C_e}}} \tag{37}$$

When $f_s = f_r$, Z_{ru} is zero, equivalent to a short circuit, resulting in a voltage gain of 1 for the FB *LLC* converter. In contrast, when $f_s = f_p$, Z_{ru} is infinite, equivalent to an open circuit, yielding a voltage gain of 0. By defining

$$k_e = \frac{C_e}{C_r}, \quad f_n = \frac{f_s}{f_r}, \quad Z_r = j\omega_s L_r + \frac{1}{j\omega_s C_r} \tag{38}$$

Z_{ru} can be normalized and rewritten as

$$Z_{ru\_n} = \frac{Z_{ru}}{Z_r} = \frac{1}{1 + k_e - k_e f_n^2} \tag{39}$$

where Z_r represents the base impedance, corresponding to the series impedance of L_r and C_r.

Fig. 19 illustrates the variation of Z_{ru_n} concerning frequency changes. Notably, as K_e increases, the deviation between Z_{ru} and Z_r becomes more pronounced, particularly at

switching frequencies higher than f_r. In other words, for the same range of switching frequency variation, Z_{ru} can provide a larger range of impedance variation compared to Z_r. This implies that the FB *LLC* converter can achieve a wider voltage gain variation range, which is advantageous for wide-voltage-range applications and light-load voltage regulation. This phenomenon has been investigated in [36][37] and will not be further extended in this paper due to the limited space. It is worth noting that the capacitors in parallel with the resonant tank in the referenced literature are additional components, whereas in this paper, C_e represents the parasitic interwinding capacitance of the transformer introduced by the SPWT configuration.

In the proposed planar transformer, C_e is estimated to be around 93 pF. The derivation process is detailed in the Appendix. Combined with the designed C_r value of 17.6 nF, k_e is calculated as 0.005, corresponding to the red curve in Fig. 19. With this small k_e, the influence of C_e on the *LLC* voltage gain can be ignored. Consequently, the voltage gain of the proposed planar transformer based FB *LLC* converter should be similar to the conventional one.

VI. Experimental Verification

A 360 W FB *LLC* converter with 180–210 V input and 12 V/30 A output is studied as a typical example. This converter is originally designed for an open-frame two-stage AC-DC power supply with a 90-264 Vac input. When the input AC voltage is in low line range (90-136 Vac), the DC bus ranges from 180 to 210 V and the *LLC* converter operates in FB mode.

Fig. 20 (a) shows the proposed FB *LLC* prototype. The main PCB in Fig. 20 (a) is also compatible for building the conventional FB *LLC* prototype by replacing the SPWT daughter card with the conventional PCB transformer daughter card as shown in Fig. 20 (b). The transformer winding arrangement and terminal connections for the proposed and conventional planar transformers are shown in Fig. 13 (a) and (c), respectively. The electrical connections within the layers of the multi-layer PCB board are established through PCB vias. Meanwhile, connections between different PCB boards are accomplished through soldering. Fig. 20 (c)-(e) provide detailed views of the transformer windings. In Fig. 20 (c) and (d), the solder joints are indicated by red rectangles, while the paths of resonant currents are highlighted by red arrows. To minimize the secondary current loops, the secondary windings are constructed using two daughter cards, each having its own SR MOSFETs. The secondary daughter cards for the conventional and proposed transformers are identical, as shown in Fig. 20 (e). Except for the planar transformer, other specifications of the conventional prototype are the same as the proposed FB *LLC* prototype, which can be found in Table V.

A. Measured Leakage Inductance

An *LCR* meter (FLUKE PM6306) is used to measure the leakage inductances at 150 kHz. The total primary leakage inductances are measured by following the methods presented in the simulation section. For the conventional transformer,

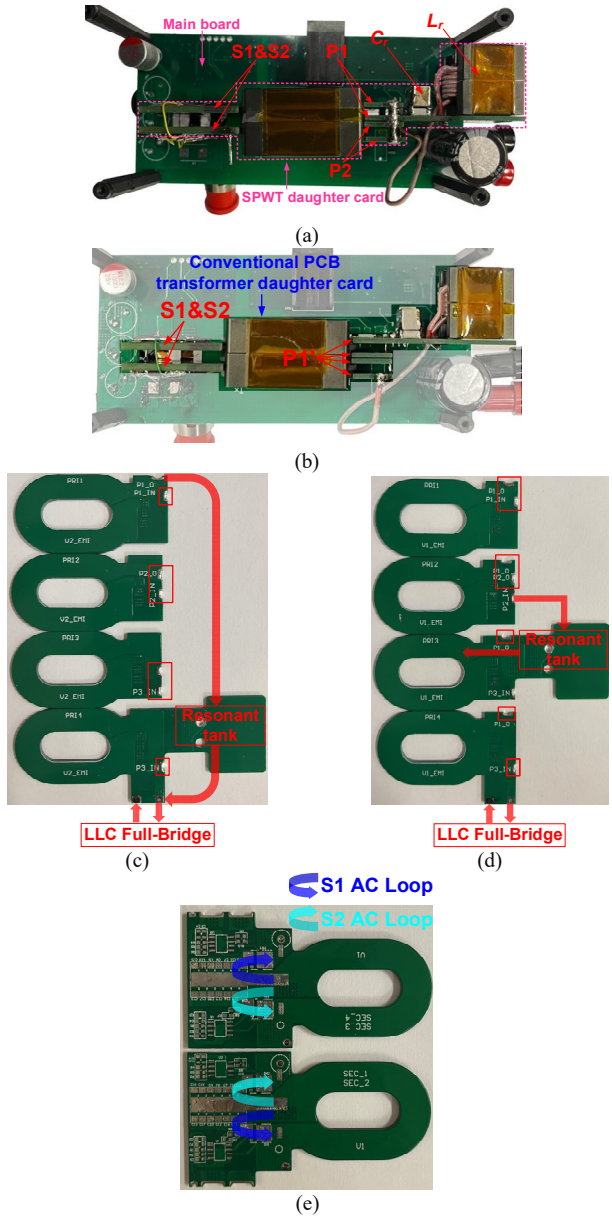


Fig. 20. Photos of prototype. (a) Proposed SPWT daughter card. (b) Conventional PCB transformer daughter card. (c) Primary windings of conventional transformer. (d) Primary windings of proposed transformer. (e) Secondary daughter cards for both conventional and proposed transformers.

TABLE V
Specifications of FB *LLC* Resonant Converter

Parameter	Value
Resonant inductor (L_r)	62 µH (3C97, PQ26/20, Ferroxcube) 24 turns (Litz 160x0.06 mm) Winding structure: 8-8-8
Resonant capacitor (C_r)	17.6 nF (C2225C222KZGACAUTO, 8 in parallel)
Resonant frequency (f_r)	152 kHz
Primary switches (Q_1~Q_4)	OSG65R125JF
Primary driver	EG3116D
Secondary SRs (SR_1, SR_2)	NTMFS5C604NLT1G
SR driver	NCP4306AAAZZZADR2G

$L_{lkP\_S1\_conv}$ is measured across the primary winding by short-circuiting secondary winding $S1$ while leaving $S2$ open. Similarly, $L_{lkP\_S2\_conv}$ is measured across the primary winding by short-circuiting secondary winding $S2$ while leaving $S1$ open. The same method is employed to measure the leakage inductances of the proposed transformer, wherein two separate primary windings, $P1$ and $P2$, were connected in series, and $L_{lkP\_S1\_prop}$ and $L_{lkP\_S2\_prop}$ are measured between winding terminals A and D.

Measured leakage inductances are provided in Table VI. It can be observed that, whether the secondary winding $S1$ is conducting or the secondary winding $S2$ is conducting, the conventional and proposed planar transformers exhibit the same total leakage inductance. Furthermore, the experimental results match well with the simulation results, with a discrepancy of only 0.04-0.06 μH. This discrepancy mainly arises from the parasitic inductance of the short-circuit connecting wires between the secondary winding terminals. This parasitic inductance can be reflected to the transformer primary side and increase the measured value of the total leakage inductance.

B. Measured Voltage Conversion Ratio and Efficiency

By sweeping the switching frequency from 135 kHz to 165 kHz, the measured voltage gain curves of the proposed and conventional prototypes are shown in Fig. 21. It can be observed that they exhibit similar voltage gain performance under both 30 A full load and 1 A light load conditions. The maximum voltage gain difference occurs at 135 kHz/1 A testing condition, where the voltage gain of the conventional prototype is only 1% lower than that of the proposed prototype. These experimental results validate the analysis presented in Section V-B that the proposed and conventional FB *LLC* prototypes should exhibit similar voltage gain performance.

The measured efficiency curves of the proposed and conventional prototypes are illustrated in Fig. 22. It can be observed that, under testing conditions ranging from 5 A light load to 30 A full load, they exhibit similar efficiency performance. The maximum efficiency difference occurs at 5 A load condition, where the efficiency of the proposed prototype is 0.07% higher than that of the conventional prototype. These experimental results validate the analysis presented in Section V-A that the use of the SPWT configuration does not introduce extra winding loss, and proposed and conventional FB *LLC* prototypes should exhibit similar efficiency performance.

C. Symmetry Verification of Proposed Planar Transformer

To validate the symmetry of the proposed planar transformer, it is necessary to extract the capacitances of the four parasitic interwinding capacitors (C_{AE}, C_{BE}, C_{CE}, and C_{DE}) associated with this transformer. The precise locations of these capacitors are shown in Fig. 4. The extraction process involves two steps:

1) Measure the capacitances of C_{P1_S} and C_{P2_S}. C_{P1_S} denotes the structural capacitance between $P1$ and the secondary windings ($S1$ and $S2$), which corresponds to the summation of C_{AE} and C_{BE}. C_{P2_S} denotes the structural capacitance between $P2$ and the secondary windings, which corresponds to the summation of C_{CE} and C_{DE}.

2) Determine the capacitance ratio K_1 (K_2) between C_{AE} and C_{P1_S} (C_{CE} and C_{P2_S}) by using a signal generator. Then, C_{AE} and C_{BE}, as well as C_{CE} and C_{DE}, can be obtained by solving (40) and (41).

$$\begin{cases} C_{P1\_S} = C_{AE} + C_{BE} \\ K_1 = \dfrac{C_{AE}}{C_{P1\_S}} \end{cases} \tag{40}$$

$$\begin{cases} C_{P2\_S} = C_{CE} + C_{DE} \\ K_2 = \dfrac{C_{CE}}{C_{P2\_S}} \end{cases} \tag{41}$$

Fig. 23 (a) illustrates the circuit connections during the measurement of C_{P1_S} and C_{P2_S}. The transformer winding terminals are short-circuited to ensure uniform electric potential within each winding. Fig. 23 (b) gives the equivalent capacitance network. Notably, C_{P1_S} and C_{P2_S} cannot be directly measured because of the existence of C_{P1_P2} (interwinding capacitor between $P1$ and $P2$). In Fig. 23 (a), the measured capacitances between M1 and M2, M1 and M3, and M2 and M3 are denoted by C_{M1_M2}, C_{M1_M3}, C_{M2_M3}, respectively. Then, the capacitances of C_{P1_S} and C_{P2_S} can be obtained by solving (42)-(44), which are both around 113 pF.

TABLE VI
MEASURED LEAKAGE INDUCTANCES (UNIT: μH)

		Measured	Simulated
Conventional	$L_{lkP\_S1\_conv}$	1.18	1.14
	$L_{lkP\_S2\_conv}$	1.19	1.13
Proposed	$L_{lkP\_S1\_prop}$	1.18	1.14
	$L_{lkP\_S2\_prop}$	1.19	1.13

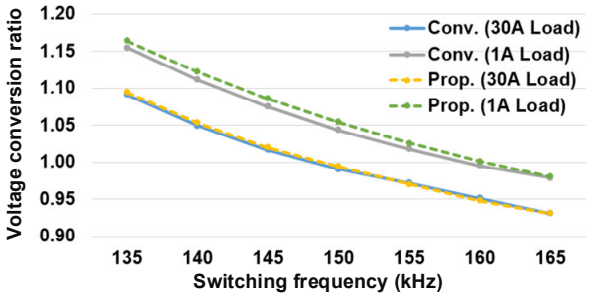


Fig. 21. Measured voltage conversion ratio.

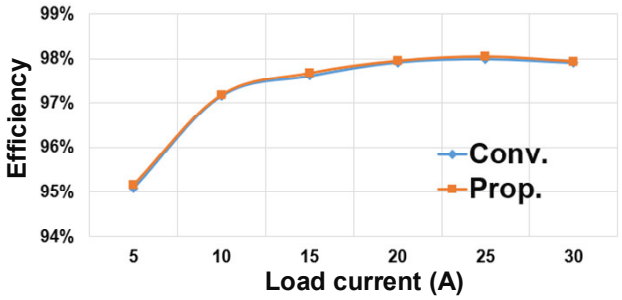
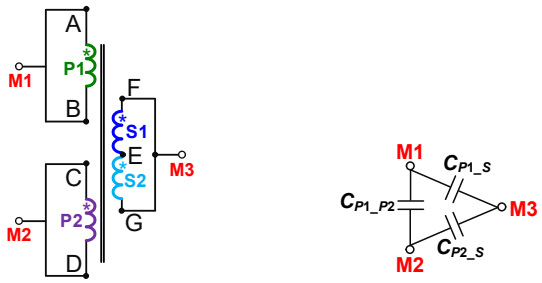
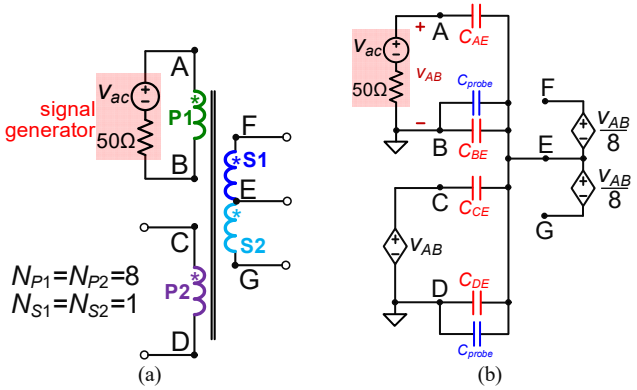


Fig. 22. Measured efficiency. V_{in} = 190 V. V_o = 12 V.



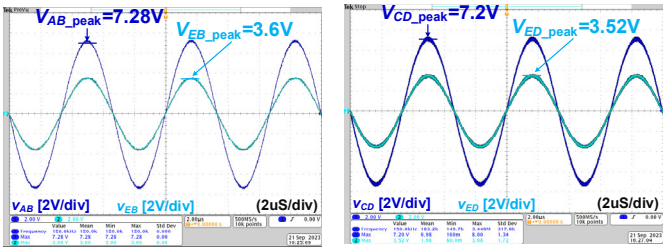
(a) (b)

Fig. 23. Measuring C_{P1_S} and C_{P2_S}. (a) Circuit connections. (b) Equivalent capacitance network.



(a) (b)

Fig. 24. Measuring K_1 and K_2. (a) Circuit connections. (b) Equivalent circuit.



(a) (b)

Fig. 25. Measured waveforms. (a) v_{AB} and v_{EB}. (b) v_{CD} and v_{ED}.

TABLE VII
MEASURED CAPACITANCES OF C_{AE}, C_{BE}, C_{CE}, AND C_{DE}

	C_{AE}	C_{BE}	C_{CE}	C_{DE}
Experimental results	58 pF	55 pF	57 pF	56 pF

$$C_{M1\_M2} = C_{P1\_P2} + \frac{C_{P1\_S}C_{P2\_S}}{C_{P1\_S}+C_{P2\_S}} \tag{42}$$

$$C_{M1\_M3} = C_{P1\_S} + \frac{C_{P1\_P2}C_{P2\_S}}{C_{P1\_P2}+C_{P2\_S}} \tag{43}$$

$$C_{M2\_M3} = C_{P2\_S} + \frac{C_{P1\_S}C_{P1\_P2}}{C_{P1\_S}+C_{P1\_P2}} \tag{44}$$

Fig. 24 (a) illustrates the method for extracting the capacitance ratios K_1 and K_2. A signal generator is applied to $P1$ winding terminals A and B, while the other winding terminals are left open. This method simulates the generation of the CM noise displacement currents via the interwinding capacitors. The equivalent circuit is given by Fig. 24 (b). By adding the sinusoidal excitation signal v_{ac} at 150 kHz, the voltage distribution along transformer windings is established. Then in Fig. 24 (b), the voltage from E to B (v_{EB}), and the voltage from A to B (v_{AB}) are measured to calculate K_1, as shown in (45). In (45), C_{probe} represents the parallel capacitance introduced by the voltage probe, which is 3.9 pF for Tektronix TPP0250. V_{EB_peak} (V_{AB_peak}) is the peak value of v_{EB} (v_{AB}). Similarly, the voltage from E to D (v_{ED}), and the voltage from C to D (v_{CD}) are measured to calculate K_2, as shown in (46). V_{ED_peak} (V_{CD_peak}) is the peak value of v_{ED} (v_{CD}).

$$\frac{V_{EB\_peak}}{V_{AB\_peak}} = \frac{C_{AE}}{C_{P1\_S}+C_{probe}} = \frac{K_1}{1+C_{probe}/C_{P1\_S}} \tag{45}$$

$$\frac{V_{ED\_peak}}{V_{CD\_peak}} = \frac{C_{CE}}{C_{P2\_S}+C_{probe}} = \frac{K_2}{1+C_{probe}/C_{P2\_S}} \tag{46}$$

Fig. 25 gives the measured waveforms of v_{AB}, v_{EB}, v_{CD}, and v_{ED}. In Fig. 25 (a), V_{EB_peak} and V_{AB_peak} are measured as 3.6 V and 7.28 V, respectively. Then, the value of K_1 can be determined by solving (45), which is around 0.512. In Fig. 25 (b), V_{ED_peak} and V_{CD_peak} are measured as 3.52 V and 7.2 V, respectively. Then, the value of K_2 can be determined by solving (46), which is around 0.506.

Substituting the values of K_1, K_2, C_{P1_S}, and C_{P2_S} into (40) and (41) allows for determining the capacitances of C_{AE}, C_{BE}, C_{CE}, and C_{DE}, which are provided in Table VII. It can be observed that the capacitances of C_{AE} and C_{BE}, as well as C_{CE} and C_{DE}, are very close. This observation verifies the symmetry of the proposed planar transformer from the CM noise perspective. In addition, Table VIII in the Appendix provides the calculated values for these four capacitances, all of which are 65 pF. These calculation results match well with the experimental results in Table VII, showing a minimal discrepancy of 8 to 10 pF. This discrepancy mainly arises from the imperfect stacking of different PCBs and insulation papers, resulting in distributed air gaps between them. Consequently, C_{P1_S} and C_{P2_S} are slightly overestimated during the calculation process, leading to the subsequent overestimations of C_{AE}, C_{BE}, C_{CE}, and C_{DE}.

D. Measured Voltage Waveforms of Transformer Winding Terminals

Fig. 26 provides the resonant tank current waveform (i_{res}), as well as the electric potential waveforms of the transformer terminals (v_a and v_b), for the conventional FB *LLC* prototype operating under full load conditions. The reference ground for v_a and v_b is PG. It is worth noting that v_a and v_b exhibit different *dv/dt* characteristics in both boost (f_s = 135 kHz < f_r) and buck (f_s = 165 kHz > f_r) mode operation range, which is consistent with the analysis in Section II. Specifically, as depicted in Fig. 26 (a), negative *dv/dt* on v_a is observed during the interval [t_{C_a}, t_{C_b}], which induces CM noise current from the secondary side to the primary side through the corresponding parasitic interwinding capacitance. During the interval [t_{C_b}, t_{C_c}], positive *dv/dt* on both v_a and v_b is observed, inducing CM noise currents from the primary side to the secondary side through the corresponding parasitic interwinding capacitance. As a result, the different *dv/dt*

This article has been accepted for publication in IEEE Journal of Emerging and Selected Topics in Power Electronics. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2024.3386654

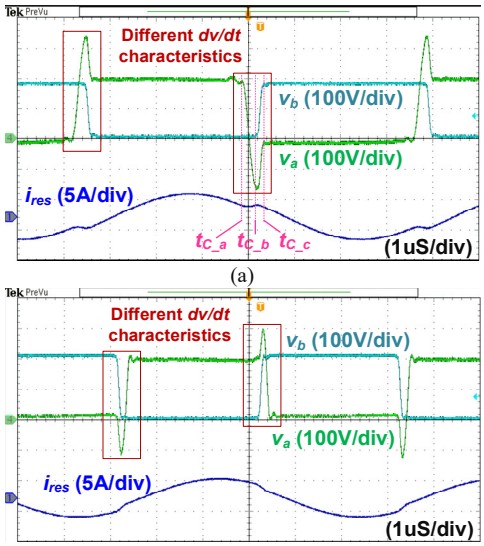


Fig. 26. Waveforms of transformer terminals in conventional FB *LLC* resonant converter under full load conditions. (a) Boost mode ($f_s < f_r$), V_{in} = 180V, f_s = 135 kHz. (b) Buck mode ($f_s > f_r$), V_{in} = 210V, f_s = 165 kHz.

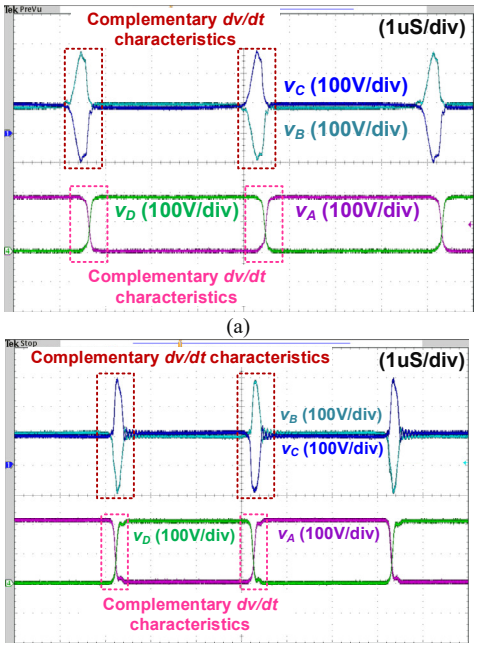


Fig. 27. Waveforms of transformer terminals in proposed FB *LLC* resonant converter under full load conditions. (a) Boost mode ($f_s < f_r$), V_{in} = 180V, f_s = 135 kHz. (b) Buck mode ($f_s > f_r$), V_{in} = 210V, f_s = 165 kHz.

characteristics of v_a and v_b generate CM noise displacement currents with different magnitudes and phases that cannot cancel each other, thereby deteriorating the CM EMI performance of the conventional *LLC* prototype. The conclusion is the same when the conventional *LLC* prototype operates above f_r.

Fig. 27 provides the voltage waveforms of the transformer terminals with respect to PG in the proposed FB *LLC* prototype under full load conditions. It is observed that v_B and v_C (v_A and v_D) have complimentary *dv/dt* characteristics in both boost and

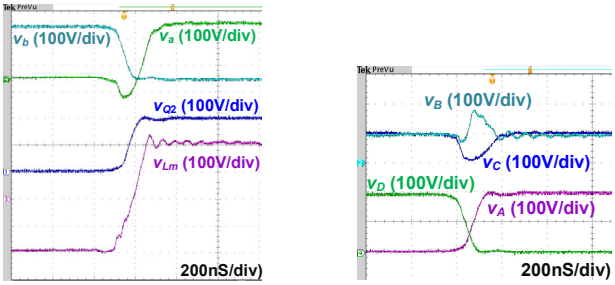


Fig. 28. Key waveforms during dead-time period when $f_s = f_r$. (a) Conventional FB *LLC* resonant converter under full load conditions. (b) Proposed FB *LLC* resonant converter under full load conditions.

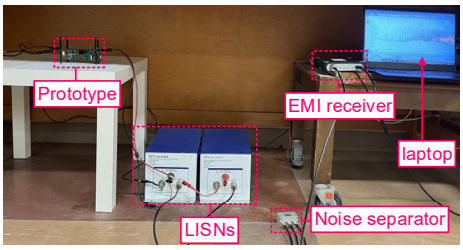


Fig. 29. Hardware setup.

buck mode operation range, which is consistent with the analysis in Section III.

When $f_s = f_r$, the impedance of the resonant tank is zero. For the conventional FB *LLC* converter, v_{Q2} (see Fig. 1) and v_a are in phase. However, due to the influence of v_{Lm} (voltage across the magnetizing inductor), the *dv/dt* of v_a and v_b exhibit different slew rates during the dead time. As illustrated in Fig. 28 (a), the *dv/dt* of v_a is slower than v_{Q2}. Consequently, the complementary nature of v_a and v_b is significantly weakened. In contrast to the conventional FB *LLC* converter, the proposed FB *LLC* converter demonstrates enhanced complementary characteristics in transformer winding terminals when $f_s = f_r$, as illustrated in Fig. 28 (b).

The complimentary *dv/dt* characteristics introduced by the proposed SPWT configuration enable the CM noise cancellation in the transformer with a symmetrical winding structure, resulting in low CM EMI noise.

E. Measured CM Noise Spectra

The hardware setup of the conducted CM EMI measurement is shown in Fig. 29. The conducted CM noise is initially measured using a LISN named LI-125C, and then separated into its CM component using a noise separator named ZSC-2-2+. The conducted CM EMI spectrum is scanned by an EMI receiver named RSA306B in accordance with the EN55032 class B standard. Fig. 30 illustrates the measured CM noise spectra (quasi-peak value) of the conventional and proposed FB *LLC* prototypes under full load conditions. The enveloping curves of the CM noise for the conventional and proposed *LLC* prototypes are depicted by dashed and solid lines, respectively. Some peaks are not connected to the enveloping curves to ensure the clear readability of the amplitude trend of the CM noise. In Fig. 30, some noise peaks occur at frequencies that are not integer

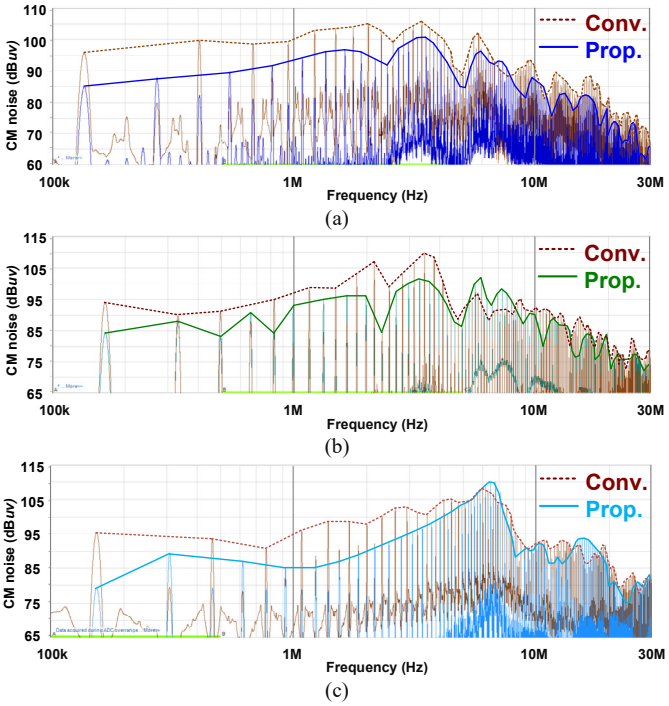


Fig. 30. Measured CM noise spectra. (a) Boost mode ($f_s < f_r$), V_{in} = 180V, f_s = 135 kHz. (b) Buck mode ($f_s > f_r$), V_{in} = 210V, f_s = 165 kHz. (c) $f_s = f_r$ = 152 kHz, V_{in} = 195V.

multiples of the switching frequency, which is attributed to background noise caused by the layout of the PCB [38]. These peaks do not affect CM noise reduction and can be resolved by appropriate PCB layout design.

The results presented in Fig. 30 show that the proposed SPWT configuration and symmetrical winding arrangement can achieve an approximately 11 dBμV reduction in CM noise for the fundamental frequencies in both boost and buck mode operation ranges of the FB *LLC* prototype. At the resonant frequency, a reduction of approximately 16 dBμV in CM noise for the fundamental frequency can be achieved. It should be noted that this CM noise attenuation is achieved without increasing the Bill of Materials (BOM) cost. However, for frequencies above 5 MHz, the reduction in CM noise is reduced due to the dominant impedance of the transformer leakage inductance. In this range, the transformer should be modeled using a complex parasitic inductance and capacitance network for CM noise analysis. Nevertheless, the CM noise remains relatively low across most of the frequency spectrum. Therefore, the proposed SPWT configuration is very effective for reducing the size of the CM EMI filter since the corner frequency of the EMI filter is determined by the noise magnitude at the fundamental frequency.

VII. Conclusion

In this paper, a low CM noise FB *LLC* converter with SPWT configuration is proposed. By placing the resonant tank between two split primary windings, the voltage across the original primary winding is redistributed and two created separate primary winding branches have complementary *dv/dt* characteristics; thus, the CM noise current generated in the transformer can be canceled completely with the symmetrical winding structure. The concept of complementary couple-turns is proposed for planar transformer applications. By choosing the overlapping primary and secondary winding turns based on the concept of complementary couple-turns, the planar transformer can be ensured to have a symmetrical winding arrangement and minimized CM noise currents before it is physically fabricated. The experimental results of a 360 W FB *LLC* converter show that the CM noise can be reduced significantly by around 16 dBμV (a reduction of around 6.3 times) at the fundamental frequency when $f_s = f_r$. The decreased CM noise allows for a reduction in the size of the CM EMI filter, which helps to improve the power density of the whole system. Importantly, it should be noted that achieving this CM noise reduction incurs no additional cost.

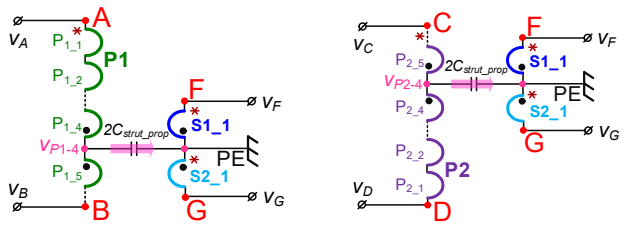


Fig. 31. (a) Lumped interwinding capacitance models of *P*1_4-*S*1_1 and *P*1_5-*S*2_1. (b) Lumped interwinding capacitance models of *P*2_4-*S*2_1 and *P*2_5-*S*1_1.

Appendix

The principle of displacement current conservation is used to derive the interwinding capacitances of the proposed planar transformer shown in Fig. 13 (a), including C_{AE}, C_{BE}, C_{CE}, C_{DE}, C_{BC}, and C_{AD}. The precise locations of these capacitors are shown in Fig. 18. In Fig. 13 (a), there are distributed interwinding capacitors within five pairs of overlapping layers, which are *P*1_4-*S*1_1, *P*1_5-*S*2_1, *P*2_4-*S*2_1, *P*2_5-*S*1_1, and *P*1_8-*P*2_8. The structural capacitance within each pair of overlapping layers remains the same. This structural capacitance is denoted as C_{strut_prop} in the following analysis.

Derivation of C_{AE}, C_{BE}, C_{CE}, and C_{DE}: Based on the one-capacitor couple-turn model, the lumped interwinding capacitance models of *P*1_4-*S*1_1, *P*1_5-*S*2_1, *P*2_4-*S*2_1, and *P*2_5-*S*1_1 are illustrated in Fig. 31. In Fig. 31 (a), black dots denotes the corresponding terminals that are used to place C_{strut_prop}. It is noted that C_{strut_prop} in *P*1_4-*S*1_1 and *P*1_5-*S*2_1 are placed at the same position and the total capacitance is $2C_{strut\_prop}$. The same applies to Fig. 31 (b).

In Fig. 31 (a), the displacement current from primary winding *P*1 to secondary windings is calculated as

$$i_{P1\_S} = 2C_{strut\_prop}\frac{dv_{P1\_4}}{dt} \tag{A1}$$

where v_{P1_4} can be derived as

$$v_{P1\_4} = v_A - 4\Delta v = v_A - \frac{v_A - v_B}{2} = \frac{v_A + v_B}{2} \tag{A2}$$

In (A2), Δv is the voltage gradient on each turn. Substituting (A2) into (A1), i_{P1_S} can be rewritten as

$$i_{P1\_S} = C_{strut\_prop}\frac{d(v_A + v_B)}{dt} \tag{A3}$$

According to the principle of displacement current conservation, the displacement current generated in C_{AE} and C_{BE} should be equal to i_{P1_S}, which can be expressed as

$$i_{P1\_S} = C_{AE}\frac{dv_A}{dt} + C_{BE}\frac{dv_B}{dt} \tag{A4}$$

By comparing (A3) and (A4), C_{AE} and C_{BE} can be derived as

$$C_{AE} = C_{BE} = C_{strut\_prop} \tag{A5}$$

The method used to derive C_{AE} and C_{BE} can similarly be applied to derive C_{CE} and C_{DE}. The specific calculation process is omitted, and C_{CE} and C_{DE} are directly provided as

$$C_{CE} = C_{DE} = C_{strut\_prop} \tag{A6}$$

Derivation of C_{AD} and C_{BC}: C_{AD} and C_{BC} primarily arise from the structural capacitance between primary winding turns $P1\_8$ and $P2\_8$. The winding-to-core capacitances are ignored due to their relatively small values. Fig. 32 provides 3D models of $P1\_8$ and $P2\_8$. x denotes the winding length direction and the overall winding length is denoted by L. The voltage distributions of $P1\_8$ and $P2\_8$ are denoted by $v_{P1\_8}(x)$ and $v_{P2\_8}(x)$ respectively. By assuming that the voltage of the winding turn is evenly distributed, $v_{P1\_8}(x)$ and $v_{P2\_8}(x)$ can be calculated by

$$\begin{cases} v_{P1\_8}(x) = v_B + \Delta v - \dfrac{\Delta v \cdot x}{L}, & x \in (0, L) \\ v_{P2\_8}(x) = v_C - \dfrac{\Delta v \cdot x}{L} = -v_B - \dfrac{\Delta v \cdot x}{L}, & x \in (0, L) \end{cases} \tag{A7}$$

The displacement current flowing from $P1\_8$ to $P2\_8$ can be calculated as

$$\begin{aligned} i_{P1\_8-P2\_8} &= \int_0^L \frac{\varepsilon_0 \varepsilon_{insul} w_{PCB}}{d_{insul}} \frac{d}{dt}\left(v_{P1\_8}(x) - v_{P2\_8}(x)\right)dx \\ &= C_{strut\_prop}\frac{d(2v_B + \Delta v)}{dt} \end{aligned} \tag{A8}$$

Since Δv is equal to $(v_A - v_B)/8$, (A8) can be rewritten as

$$i_{P1\_8-P2\_8} = C_{strut\_prop}\frac{d}{dt}\left(\frac{v_A + 15v_B}{8}\right) \tag{A9}$$

Based on the principle of displacement current conservation, the displacement current generated in C_{BC} and C_{AD} should be equal to $i_{P1\_8\text{-}P2\_8}$, which is expressed as

$$\begin{aligned} i_{P1\_8-P2\_8} &= C_{AD}\frac{d(v_A - v_D)}{dt} + C_{BC}\frac{d(v_B - v_C)}{dt} \\ &= 2C_{AD}\frac{dv_A}{dt} + 2C_{BC}\frac{dv_B}{dt} \end{aligned} \tag{A10}$$

By comparing (A9) and (A10), C_{AD} and C_{BC} can be derived as

$$\begin{cases} C_{AD} = C_{strut\_prop}/16 \\ C_{BC} = 15C_{strut\_prop}/16 \end{cases} \tag{A11}$$

The capacitance C_e can be calculated by

$$C_e = C_{BC} + \frac{C_{BE}C_{CE}}{C_{BE} + C_{CE}} = 23C_{strut\_prop}/16 \tag{A12}$$

The calculation results are summarized in Table VIII.

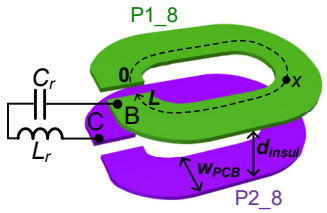


Fig. 32. 3D models of $P1\_8$ and $P2\_8$.

TABLE VIII
INTERWINDING CAPACITANCES OF PROPOSED PLANAR TRANSFORMER

	C_{AE}, C_{BE}, C_{CE}, C_{DE}	C_{AD}	C_{BC}	C_e
Calculation results	65 pF	4 pF	61 pF	93 pF

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