Common-Mode Noise Reduction in Full-Bridge *LLC* Resonant Converter with Split Primary Winding Transformer

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***Abstract*— This paper addresses the issue of common-mode (CM) conducted electromagnetic interference (EMI) noise in full-bridge (FB) *LLC* resonant converters. In conventional FB *LLC* resonant converters, the position of the resonant tank can affect the symmetry of the entire circuit, leading to different *dv/dt* values at the two winding terminals of the transformer. This results in non-cancelable displacement currents generated in the parasitic interwinding capacitance of the transformer, leading to severe CM noise issues. In this paper, a low CM noise FB *LLC* resonant converter with the Split Primary Winding Transformer (SPWT) configuration is proposed. The transformer primary winding is split into two windings and the resonant tank is connected between these two windings. With a symmetrical winding structure, the CM noise current generated in the transformer can be canceled completely. The concept of complementary couple-turns is proposed to ensure a symmetrical winding arrangement for the planar transformer in the printed circuit board (PCB) layout stage before it is fabricated physically. A 360 W FB *LLC* prototype with a planar transformer is built to verify the feasibility and validity of the proposed methods. The CM noise is reduced by around 11 dBμV (a reduction of around 4 times) below 5 MHz.**

Keywords—Split Primary Winding Transformer (SPWT), Full-Bridge (FB), LLC resonant converter, Common-Mode (CM) noise, Planar transformer

I. INTRODUCTION

The FB *LLC* resonant converter has been widely used in medium-to-high power applications because of its simple structure, high cost-effectiveness, and soft-switching capability [1]-[3]. The FB *LLC* converter possesses a natural symmetrical structure, which yields a pair of switching nodes having complementary electric potentials with respect to the ground. When the associated parasitic capacitances of these nodes are equal, the generated CM noise displacement currents can be completely cancelled by each other. However, the voltage across the resonant tank affects the electric potentials of the transformer's primary winding terminals, which generates a large CM noise displacement current in the interwinding capacitance of the transformer [4]. This issue is particularly severe in planar transformers, which have a larger parasitic interwinding capacitance than traditional wire-wound transformers due to the larger overlapping area between adjacent winding layers [5][6]. The combination of large parasitic interwinding capacitance and large *dv/dt* difference leads to severe CM noise problems.

Various methods have been proposed to suppress the CM noise current flowing through the transformer of isolated power converters [7]-[24]. The shielding technique is widely used to block the electric coupling between the transformer primary and secondary windings [7]-[12]. However, there is a large conduction loss in shielding layers because of the eddy current, which results in lower converter efficiency. In [13]-[15], the overlapping primary and secondary winding layers of the transformer are made to have the same voltage distributions. There is no CM noise displacement current in the interwinding capacitance because of zero *dv/dt*. But this approach does not work for FB *LLC* converters since there are no static points in transformer primary winding terminals. The CM noise current cannot be completely canceled. In [16], a static-point connection is proposed to establish the static points at the primary winding, so as to build the paired winding layers with the same *dv/dt*. However, it is hard to implement this approach in medium-to-high power applications with planar transformers. Especially for the high turns ratio planar transformer with an interleaving winding structure, too many paired layers are needed to maintain zero *dv/dt* between primary and secondary winding layers, which results in high manufacture cost and large transformer size. Passive components and extra transformer winding can be used to cancel the CM noise current in [17]-[24]. In [17]-[20], balanced resonant tanks are utilized for the CM noise reduction of FB *LLC* converters. Each resonant inductor and capacitor are separated into two components with the same value. The balance condition is sensitive to the components' tolerance. CM noise cancellation capacitor is added to the transformer in [21]-[23]. The capacitor value is selected based on the calculation or experimental results of the transformer's equivalent interwinding capacitance. In [24], an antiphase winding is introduced to generate the out-of-phase CM noise current. Although the CM noise performance can be improved, extra components or transformer windings are needed which increases the cost and decreases the power density of the converter.

In this paper, the Split Primary Winding Transformer (SPWT) configuration is proposed for FB *LLC* converters to reduce the CM noise. The proposed SPWT approach offers a

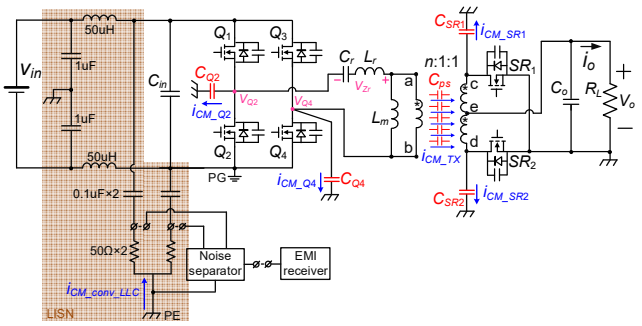


Fig. 1. CM noise propagation paths of conventional FB *LLC* resonant converter.

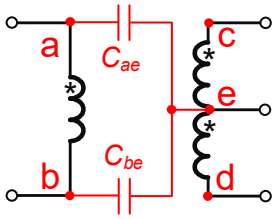


Fig. 2. Lumped interwinding capacitance mode of transformer in conventional FB *LLC* resonant converter.

simple and cost-effective solution for reducing CM noise in the FB *LLC* converter without using any additional components.

II. CM Noise Analysis of Conventional FB *LLC* Resonant Converter

Fig. 1 depicts the CM noise propagation paths of the conventional FB *LLC* converter. During the conducted EMI measurement, the secondary ground (SG) is connected to the protective earth (PE). The CM noise currents generated by the switching nodes will couple into the PE via parasitic capacitances, which can be detected by the line impedance stabilization network (LISN). The LISN, as a passive network, serves the purpose of isolating the testing system with a reference impedance and providing measurement points to the EMI receiver. A noise separator is utilized to effectively separate the original conducted EMI noise into its CM noise component.

As shown in Fig. 1, on the secondary side, i_{CM_SR1} and i_{CM_SR2} denote the CM noise currents generated by the secondary-side voltage pulsation nodes on the circuit-to-PE parasitic capacitors (C_{SR1} and C_{SR2}). Since SG is connected to PE, they circulate back through SG instead of LISN. Hence, i_{CM_SR1} and i_{CM_SR2} do not contribute to the total CM noise and can be ignored.

Typically, the magnitude of the current passing through the LISN is in the range of microamperes to milliamperes. In particular, a CM current of 40 μA at 150 kHz (which translates to 66 dBμV when flowing into 50 Ω) exceeds the limits specified by EN55032 Class B (quasi-peak value). Therefore, the *dv/dt* of the LISN can be considered negligible compared to that of the converter's voltage pulsation nodes, and the primary ground (PG) can be treated as equivalently connected to PE from the perspective of CM noise coupling. On the primary side, C_{Q2} (C_{Q4}) is the parasitic capacitor between the drain of MOSFET Q_2 (Q_4) and PE. By using PE as the reference point, the electric potentials of primary phase-leg midpoints are denoted by v_{Q2} and v_{Q4}. The CM noise currents generated in C_{Q2} and C_{Q4} are denoted by i_{CM_Q2} and i_{CM_Q4}, respectively. Given the symmetrical layouts of the two primary phase legs and the consistent packaging of the MOSFETs, C_{Q2} can be considered as equal to C_{Q4}. Since Q_2 and Q_4 are switched at 50% duty and 180 degrees out of phase with each other, v_{Q2} and v_{Q4} have complimentary *dv/dt* characteristics. When v_{Q2} has a positive *dv/dt*, v_{Q4} will have a negative *dv/dt* with the same amplitude. Therefore, i_{CM_Q2} and i_{CM_Q4} will be canceled by each other. i_{CM_Q2} and i_{CM_Q4} are removed from the following CM noise analysis.

According to the above analysis, the total CM noise current $i_{CM\_conv\_LLC}$ is dominated by i_{CM_TX}. i_{CM_TX} represents the total CM noise displacement current flowing through the distributed interwinding capacitance C_{ps} of the transformer. i_{CM_TX} is related to the electric potentials of the transformer winding terminals and parasitic interwinding capacitance of the transformer. In order to quantitatively analyze i_{CM_TX}, the parasitic interwinding capacitance model of the transformer has been developed. By ignoring the effect of the transformer's leakage inductance, the two-capacitor model can be used to characterize the interwinding capacitance of a center-tapped three-winding transformer [22]. As shown in Fig. 2, C_{ae} and C_{be} are used to model the lumped interwinding capacitors of the transformer. Since the winding terminal *e* is connected to the dc output, the corresponding *dv/dt* can be treated as zero. Thus, i_{CM_TX} can be calculated by (1), where v_a and v_b denote the electric potentials of transformer primary winding terminals *a* and *b* with respect to PE. When a transformer is constructed, the values of C_{ae} and C_{be} are then determined. v_a and v_b will vary with different operation conditions of the *LLC* converter, and then influence the CM EMI performance of the whole system.

$$i_{CM\_TX} = C_{ae}\frac{dv_a}{dt} + C_{be}\frac{dv_b}{dt} \tag{1}$$

In Fig. 1, since winding terminal *b* is connected to the drain of MOSFET Q_4, v_b is consistent with v_{Q4} which is a typical trapezoidal wave. v_a is equal to $v_{Q2} + v_{Zr}$, where v_{Zr} denotes the voltage across the resonant tank. So, (1) can be rewritten as shown in (2), where dv_{Q2}/dt is substituted by $-dv_{Q4}/dt$ since v_{Q2} and v_{Q4} have complementary *dv/dt* characteristics. If the transformer is made symmetrically, the values of C_{ae} and C_{be} can be treated as equal; then the influence of dv_{Q4}/dt on i_{CM_TX} can be eliminated. However, the influence of v_{Zr} still exists.

$$\begin{aligned} i_{CM\_TX} &= C_{ae}\frac{d(v_{Q2}+v_{Zr})}{dt} + C_{be}\frac{dv_{Q4}}{dt} \\ &= (C_{be}-C_{ae})\frac{dv_{Q4}}{dt} + C_{ae}\frac{dv_{Zr}}{dt} \end{aligned} \tag{2}$$

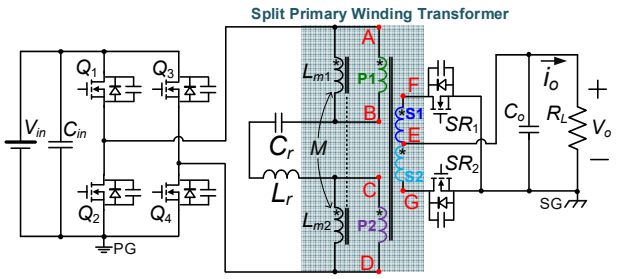


Fig. 3. FB *LLC* resonant converter with SPWT configuration.

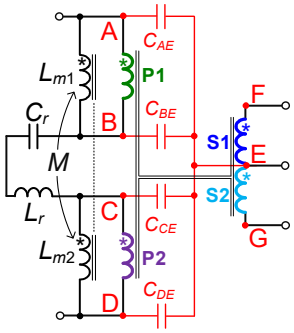


Fig. 4. Lumped interwinding capacitance model of transformer in proposed FB *LLC* resonant converter.

In conclusion, the placement of the resonant tank between the midpoint of the primary phase leg and transformer winding terminal *a* introduces an additional CM noise voltage variable, v_{Zr}. v_a and v_b will exhibit different *dv/dt* characteristics because of the influence of v_{Zr}. The CM noise displacement currents generated by v_a and v_b cannot be canceled with a symmetrical transformer winding arrangement. And CM noise is not minimized. In order to reduce the CM noise in the conventional FB *LLC* converter, the displacement currents generated by v_a and v_b via the corresponding parasitic interwinding capacitors should be eliminated.

III. SPWT Configuration for FB *LLC* Resonant Converter

A. Proposed SPWT configuration

Fig. 3 shows the circuit diagram of the FB *LLC* converter with the SPWT configuration. Compared to conventional FB *LLC* converters, the transformer's primary winding is split into two separate windings *P*1 and *P*2. The split two primary windings *P*1 and *P*2 have the same number of turns. The resonant inductor L_r and resonant capacitor C_r are placed between the primary windings *P*1 and *P*2. L_{m1} (L_{m2}) denotes the magnetizing inductance seen from the primary winding *P*1 (*P*2). *M* denotes the mutual inductance of L_{m1} and L_{m2}. The total primary side magnetizing inductance L_{m_SPWT} is calculated as

$$L_{m\_SPWT} = L_{m1} + L_{m2} + 2M \tag{3}$$

The CM noise model of the proposed FB *LLC* converter has been developed to better illustrate the cancellation mechanism of CM noise displacement currents. First, the input

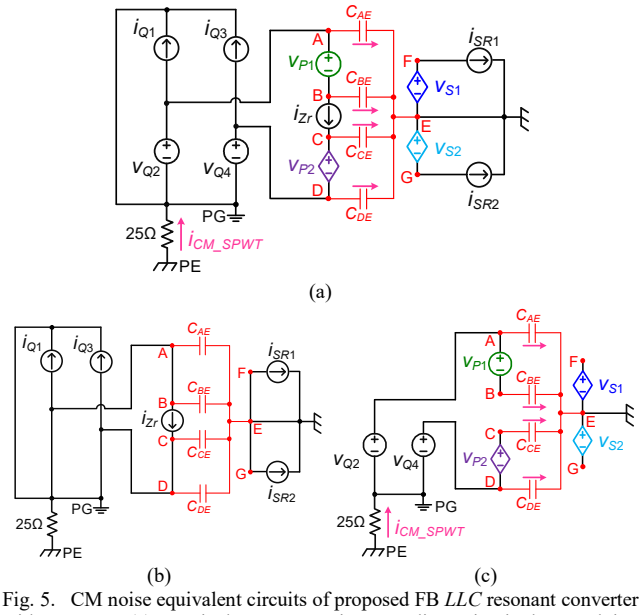


Fig. 5. CM noise equivalent circuits of proposed FB *LLC* resonant converter with SPWT. (a) Equivalent CM noise coupling circuit by applying substitution theory. (b) Decoupled CM noise equivalent circuit with current noise sources. (c) Decoupled CM noise equivalent circuit with voltage noise sources.

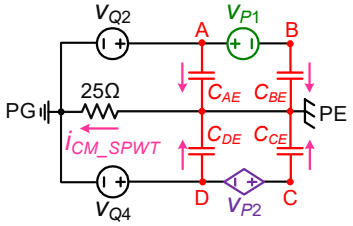


Fig. 6. Simplified CM noise coupling circuit of proposed FB *LLC* resonant converter.

and output dc capacitors are treated as a short circuit within conducted EMI frequency range and LISN is characterized as a 25-Ω resistor. Based on the two-capacitor transformer winding capacitance model [22], C_{AE} and C_{BE} (C_{CE} and C_{DE}) are used to model the lumped interwinding capacitors between the secondary windings and the primary winding *P*1 (*P*2), as shown in Fig. 4. It is noted that the interwinding capacitance between *P*1 and *P*2 does not introduce the CM noise current as the displacement current generated in that capacitance is confined within the transformer primary side. Then, the remaining circuit elements in Fig. 3 are replaced with CM noise sources by using superposition theory. Q_1, Q_3, SR_1, SR_2, and resonant tank are substituted with current sources with their own current waveforms, which are denoted by i_{Q1}, i_{Q3}, i_{SR1}, i_{SR2}, and i_{Zr} respectively. Q_2, Q_4, and primary winding *P*1 are substituted with voltage sources with their own voltage waveforms, which are denoted by v_{Q2}, v_{Q4}, and v_{P1} respectively. Based on the transformer turns ratio, all other transformer windings are substituted with voltage-controlled voltage sources v_{P2}, v_{S1}, and v_{S2}. Since L_{m1} and L_{m2} are in parallel with voltage sources v_{P1} and v_{P2}, they are ignored in the CM noise

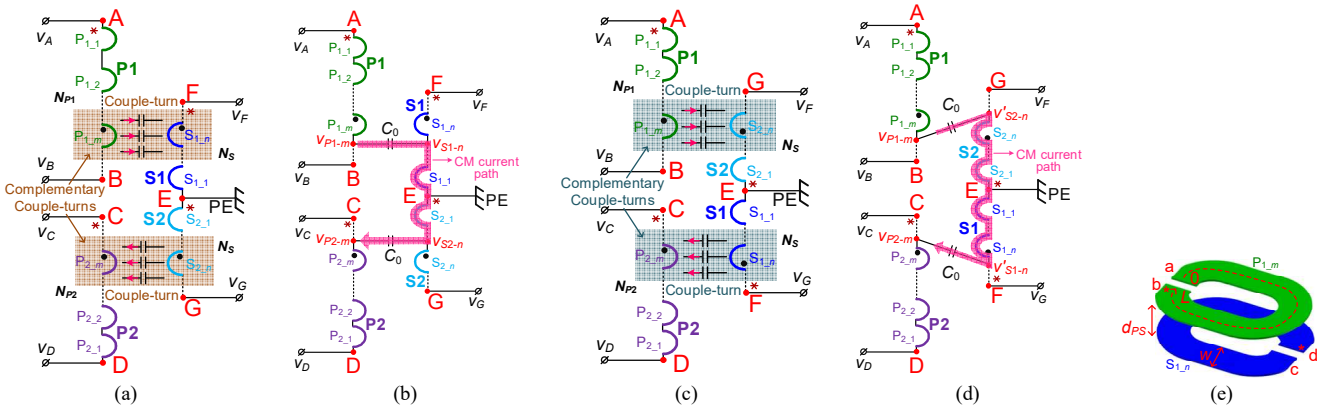


Fig. 7. Mechanism of CM noise displacement current cancellation for symmetrical planar transformer with SPWT configuration. (a) Distributed capacitances in couple-turns *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n*. (b) Lumped capacitance models for couple-turns *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n*. (c) Distributed capacitances in couple-turns *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n*. (d) Lumped capacitance models for couple-turns *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n*. (e) 3D model of couple-turn *P*1_*m*-*S*1_*n*.

analysis. Finally, the CM noise model of the proposed FB *LLC* converter is obtained, as shown in Fig. 5 (a).

Superposition theory is used to simplify the circuit shown in Fig. 5 (a). When analyzing one noise source, the other voltage sources are considered as short circuits and current sources are considered as open circuits. Fig. 5 (b) and (c) give the decoupled CM noise equivalent circuits with current and voltage noise sources, respectively. In Fig. 5 (b), the current sources i_{Q1}, i_{Q3}, i_{SR1}, i_{SR2}, and i_{Zr} are short-circuited, which are ignored. In Fig. 5 (c), v_{S1} and v_{S2} are open, which do not generate any CM noise currents. There are four remaining CM noise sources that are v_{Q2}, v_{Q4}, v_{P1}, and v_{P2}, respectively. Based on the above analysis, Fig. 6 gives the simplified CM noise coupling circuit of the proposed FB *LLC* converter.

Based on Fig. 6, the total CM noise currents can be calculated by (4). v_A, v_B, v_C, and v_D denote the electric potentials of transformer primary winding terminals with respect to PE, which are given in (5). As v_{Q2} and v_{Q4} are complementary (i.e., $v_{Q2} = -v_{Q4}$), it follows that v_A and v_D are also complementary (i.e., $v_A = -v_D$). Furthermore, since the split two primary windings have the same number of turns, by ignoring the leakage inductance, $v_{P1} = v_{P2}$. Thus, $v_B = v_{Q2} - v_{P1} = -v_{Q4} - v_{P2}$, which implies v_B and v_C are also complementary (i.e., $v_B = -v_C$). Based on this, (4) can be rewritten by (6). It is observed that i_{CM_SPWT} can be fully canceled if the transformer is made symmetrically, which means $C_{AE} = C_{DE}$ and $C_{BE} = C_{CE}$. As a result, the CM noise current generated in C_{AE} can be canceled by that generated in C_{DE}, and the CM noise current generated in C_{BE} can be canceled by that generated in C_{CE}, thereby resulting in a net CM noise current of zero.

$$i_{CM\_SPWT} = C_{AE}\frac{dv_A}{dt} + C_{DE}\frac{dv_D}{dt} + C_{BE}\frac{dv_B}{dt} + C_{CE}\frac{dv_C}{dt} \tag{4}$$

$$\begin{cases} v_A = v_{Q2} \\ v_B = v_{Q2} - v_{P1} \\ v_C = v_{Q4} + v_{P2} \\ v_D = v_{Q4} \end{cases} \tag{5}$$

$$i_{CM\_SPWT} = (C_{AE} - C_{DE})\frac{dv_A}{dt} + (C_{BE} - C_{CE})\frac{dv_B}{dt} \tag{6}$$

As discussed above, achieving a symmetrical winding configuration is crucial for effectively reducing the CM noise displacement current generated in the transformer interwinding capacitance when utilizing the SPWT configuration. Specifically, the symmetrical condition refers to the equality of C_{AE} and C_{DE} as well as C_{BE} and C_{CE}.

B. Design of symmetrical winding arrangement for Planar Transformer

Symmetrical winding structure is critical to apply SPWT method for fully cancelling the CM noise displacement current generated in the transformer interwinding capacitance. Fig. 7 (a) gives distributed interwinding capacitance model of a center-tapped four-winding planar transformer with proposed SPWT configuration. N_s denotes the turns number of secondary windings *S*1 and *S*2. N_{P1} and N_{P2} denote the turns number of primary windings *P*1 and *P*2, respectively. P_{1_m} (P_{2_m}) is defined as the *m*th primary winding turn of *P*1 (*P*2) from terminal *A* (*D*). S_{1_n} (S_{2_n}) is defined as the *n*th secondary winding turn of *S*1 (*S*2) from terminal *E*. Couple-turn denotes a pair of overlapping winding turns that belong to the primary and secondary winding respectively. According to the one-capacitor couple-turn model derived in [23], from the CM noise perspective, the parasitic physical interwinding capacitance of the couple-turn can be equivalently placed between a pair of corresponding terminals. Based on this, Fig. 7 (b) gives the lumped interwinding capacitance model of couple-turns in Fig. 7 (a). Since the impedance of the winding turn resistance is much smaller than that of the inductance, the voltage difference between any two adjacent winding turns can be considered as a constant Δv. v_{P1_m}, v_{P2_m}, v_{S1_n} and v_{S1_n} in Fig. 7 (b) can be calculated as shown in (7)-(10). The CM noise currents generated in couple-turns *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n* can be calculated as shown in (11) and (12), by assuming a constant parasitic physical interwinding capacitance C_0 of each couple-turn. Fig. 7 (e) gives the 3D model of couple turn *P*1_*m*-*S*1_*n*, and C_0 can be calculated as

shown in (13). $\varepsilon_{\text{Insul}}$ denotes the permittivity of the insulation material, d_{PS} denotes the distance between two winding turns, L and w denote the length and width of the winding turns. Based on (11) and (12), it is observed that couple-turns *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n* have complementary CM noise displacement currents that can be canceled by each other. In this paper, *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n* are defined as a pair of complementary couple-turns.

$$v_{P1\_m} = v_A - m\Delta v \tag{7}$$

$$v_{P2\_m} = v_D + m\Delta v \tag{8}$$

$$v_{S1\_n} = (n-1)\Delta v \tag{9}$$

$$v_{S2\_n} = -(n-1)\Delta v \tag{10}$$

$$i_{CM\_P1\_m-S1\_n} = C_0 \frac{d(v_A - (m+n-1)\Delta v)}{dt} \tag{11}$$

$$i_{CM\_P2\_m-S2\_n} = C_0 \frac{d(v_D + (m+n-1)\Delta v)}{dt} \tag{12}$$

$$C_0 = \varepsilon_0 \varepsilon_{\text{Insul}} \frac{w \cdot L}{d_{PS}} \tag{13}$$

Likewise, based on Fig. 7 (c) and (d), the CM noise displacement currents generated in couple-turns *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n* are given in (14) and (15), which are also complementary. Hence, *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n* are also a pair of complementary couple-turns.

$$i_{CM\_P1\_m-S2\_n} = C_0 \frac{d(v_A - (m-n)\Delta v)}{dt} \tag{14}$$

$$i_{CM\_P2\_m-S1\_n} = C_0 \frac{d(v_D + (m-n)\Delta v)}{dt} \tag{15}$$

Based on the previous analysis, the planar transformer winding arrangement can be symmetrical from the CM noise perspective and the total CM noise displacement current generated in the planar transformer can be fully canceled when the following two conditions are satisfied:

1) Overlapping layers should be selected based on the concept of complementary couple-turns. There are two types of complementary couple-turns: *P*1_*m*-*S*1_*n* and *P*2_*m*-*S*2_*n*, as well as *P*1_*m*-*S*2_*n* and *P*2_*m*-*S*1_*n*. Definitions for *P*1_*m*-*S*1_*n*, *P*2_*m*-*S*2_*n*, *P*1_*m*-*S*2_*n*, and *P*2_*m*-*S*1_*n* are provided in Fig. 7 for the center-tapped transformer structure.

If the *m*th winding turn of *P*1 is overlapped with the *n*th winding turn of *S*1, the *m*th winding turn of *P*2 needs to be overlapped with the *n*th winding turn of *S*2 so as to generate the complementary CM noise current. Likewise, If the *m*th winding turn of *P*1 is overlapped with the *n*th winding turn of *S*2, the *m*th winding turn of *P*2 needs to be overlapped with the *n*th winding turn of *S*1.

2) The complementary couple-turns should be designed to have the same parasitic structural interwinding capacitances.

IV. Experimental Verification

A 360 W FB *LLC* converter with 180–210 V input and 12 V/30 A output is studied as a typical example. The transformer

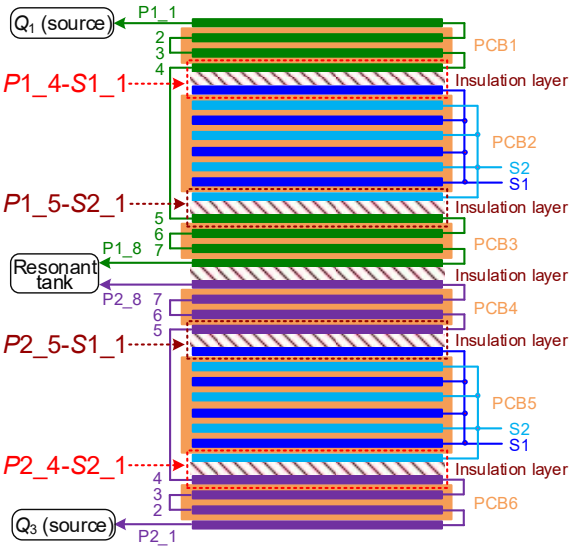


Fig. 8. Transformer winding arrangement and terminal connections of proposed FB *LLC* resonant converter. Refer Fig. 3 for locations of Q_1 (source), Q_3 (source), and resonant tank.

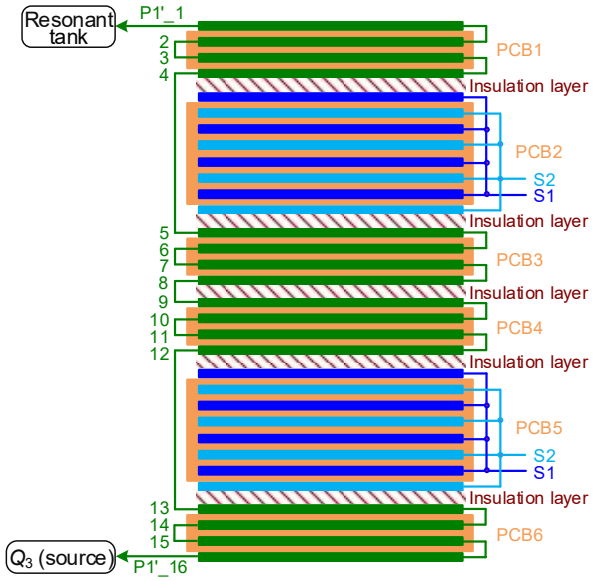


Fig. 9. Transformer winding arrangement and terminal connections of conventional FB *LLC* resonant converter. Refer Fig. 1 for locations of Q_3 (source) and resonant tank.

turns ratio used in the prototype is 16:1:1. DMR96 ferrite core material from DMEGC is selected and the core size is ECW34C (customized from DMEGC).

Fig. 8 illustrates the winding arrangement and terminal connections of the proposed planar transformer. The transformer windings are designed with one turn per layer with the same width. A partially interleaving structure is used to reduce the leakage inductance and winding AC resistance. The primary windings are designed with 4 pieces of 4-layer 4OZ PCB. The secondary windings are designed with 2 pieces of 8-layer 4OZ PCB. Two pairs of complementary couple-turns are

selected for the overlapping layers, which are *P*1_4-*S*1_1 and *P*2_4-*S*2_1, *P*1_5-*S*2_1, and *P*2_5-*S*1_1. Since 6 PCBs are stacked by using the same type of insulation material with the same thickness, the complementary couple-turns have the same parasitic structural interwinding capacitances. Thus, this planar transformer is symmetrical from the CM noise perspective and the total CM noise displacement current should be significantly reduced.

For comparison, Fig. 9 illustrates the transformer winding arrangement and terminal connections of the conventional FB *LLC* converter. It is noted that the conventional planar transformer has the same winding arrangement as the proposed planar transformer in Fig. 8, but the terminal connections are different. For the conventional planar transformer, there is only one primary winding which is denoted by *P*1'. *P*1'_1 is the first primary winding turn which is connected to the resonant tank. *P*1'_16 is the last primary winding turn which is connected to Q_3 (Source) in Fig. 1. The magnetizing inductance seen from *P*1' is measured as 177 μH, which is identical with L_{m_SPWT} of the proposed planar transformer. Other specifications of the conventional prototype are the same as the proposed *LLC* prototype, which can be found in Table I.

TABLE I
SPECIFICATIONS OF PROPOSED FB *LLC* RESONANT CONVERTER

Parameter	Value
Resonant inductor (L_r)	62 μH (3C97, PQ26/20, TDK)
Resonant capacitor (C_r)	C2225C222KZGACAUTO (2.2 nF, 8 in parallel)
Resonant frequency (f_r)	152 kHz
Primary switches (Q_1~Q_4)	OSG65R125JF
Secondary SRs (SR_1, SR_2)	NTMFS5C604NLT1G

A. *Measured Voltage Waveforms of Transformer Winding Terminals*

Fig. 10 provides the resonant tank current waveform (i_{res}), as well as the electric potential waveforms of the transformer terminals (v_a and v_b), for the conventional FB *LLC* converter prototype operating under full load conditions. It is worth noting that v_a and v_b exhibit different *dv/dt* characteristics in both boost (f_s = 135 kHz < f_r) and buck (f_s = 165 kHz > f_r) mode operation range, which is consistent with the analysis in Section II. Specifically, as depicted in Fig. 10 (a), negative *dv/dt* on v_a is observed during the interval [t_{C_a}, t_{C_b}], which induces CM noise current from the secondary side to the primary side through the corresponding parasitic interwinding capacitance. During the interval [t_{C_b}, t_{C_c}], positive *dv/dt* on both v_a and v_b is observed, inducing CM noise currents from the primary side to the secondary side through the corresponding parasitic interwinding capacitance. As a result, the different *dv/dt* characteristics of v_a and v_b generate CM noise displacement currents with different magnitudes and phases that cannot cancel each other, thereby deteriorating the CM EMI performance of the conventional *LLC* converter prototype. The conclusion is the same when the *LLC* converter prototype operates above f_r.

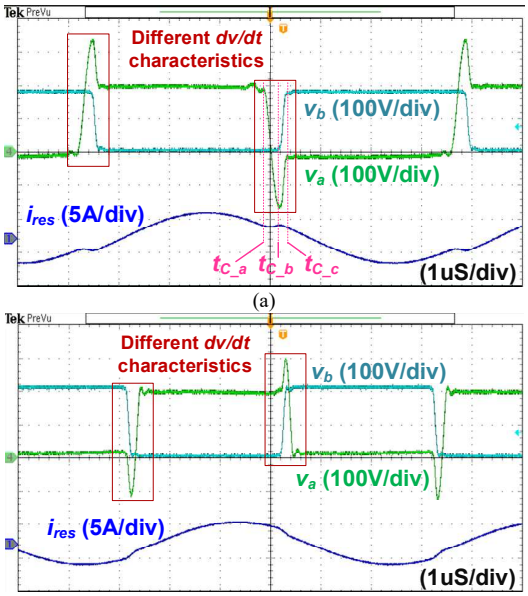


Fig. 10. Waveforms of transformer terminals in conventional FB *LLC* resonant converter under full load conditions. (a) Boost mode ($f_s < f_r$), V_{in} = 180V, f_s = 135 kHz. (b) Buck mode ($f_s > f_r$), V_{in} = 210V, f_s = 165 kHz.

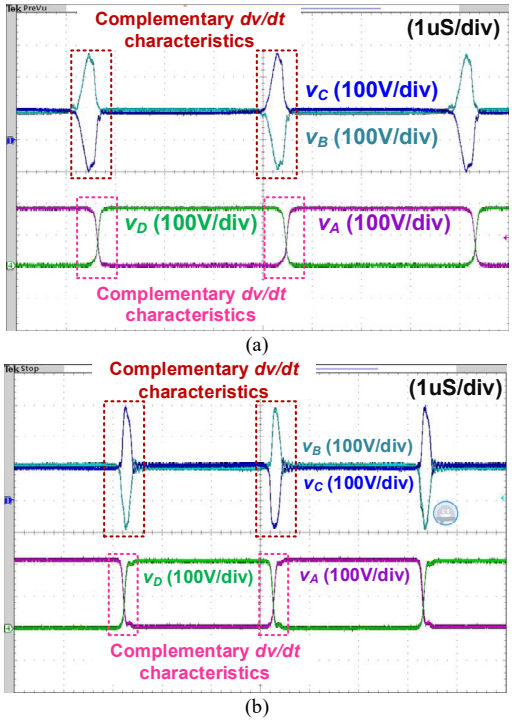


Fig. 11. Waveforms of transformer terminals in proposed FB *LLC* resonant converter under full load conditions. (a) Boost mode ($f_s < f_r$), V_{in} = 180V, f_s = 135 kHz. (b) Buck mode ($f_s > f_r$), V_{in} = 210V, f_s = 165 kHz.

Fig. 11 provides the waveforms of transformer terminals in the proposed FB *LLC* converter prototype under full load conditions. It is observed that v_B and v_C (v_A and v_D) have complimentary *dv/dt* characteristics in both boost and buck mode operation range, which is consistent with the analysis in

Section III. These complimentary *dv/dt* characteristics enable the cancellation of CM noise in the transformer with a symmetrical winding structure, resulting in low CM EMI noise.

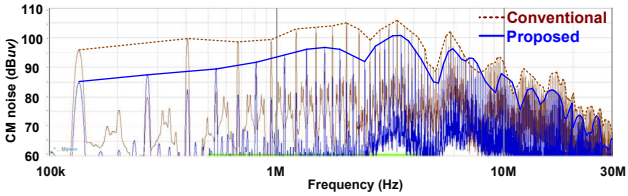
B. Measured CM Noise Spectra

The conducted EMI noise is initially measured using a LISN named LI-125C, and then separated into its CM component using a noise separator named ZSC-2-2+. The conducted CM EMI spectrum is scanned by an EMI receiver named RSA306B in accordance with the EN55032 class B standard. Fig. 12 illustrates the measured CM noise spectra (quasi-peak value) of the conventional and proposed FB *LLC* converters under full load conditions. The enveloping curves of the CM noise for the conventional and proposed *LLC* converters are depicted by dashed and solid lines, respectively. Some peaks are not connected to the enveloping curves to ensure the clear readability of the amplitude trend of the CM noise. In Fig. 12, some noise peaks occur at frequencies that are not integer multiples of the switching frequency, which is attributed to background noise caused by the layout of the PCB [25]. These peaks do not affect CM noise reduction and can be resolved by appropriate PCB layout design.

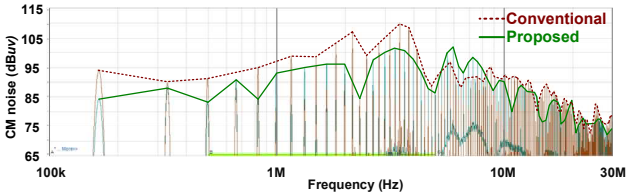
The results presented in Fig. 12 show that the proposed SPWT configuration and symmetrical winding arrangement can achieve an approximately 11 dBμV reduction in CM noise for the fundamental frequencies in both boost and buck mode operation ranges of the FB *LLC* prototype. It should be noted that this CM noise attenuation is achieved without increasing the Bill of Materials (BOM) cost. However, for frequencies above 5 MHz, the reduction in CM noise is reduced due to the dominant impedance of the transformer leakage inductance. In this range, the transformer should be modeled using a complex parasitic inductance and capacitance network for CM noise analysis. Nevertheless, the CM noise remains relatively low across most of the frequency spectrum. Therefore, the proposed SPWT configuration is very effective for reducing the size of the CM EMI filter since the corner frequency of the EMI filter is determined by the noise magnitude at the fundamental frequency.

V. Conclusions

In this paper, a low CM noise FB *LLC* converter with SPWT configuration is proposed. By placing the resonant tank between two split primary windings, the voltage across the original primary winding is redistributed and two created separate primary winding branches have complementary *dv/dt* characteristics; thus, the CM noise current generated in the transformer can be canceled completely with the symmetrical winding structure. Compared with the conventional FB *LLC* converter, the influence of the resonant tank on the CM noise current generated in the transformer can be eliminated and the total CM noise current can be minimized without any additional cost. By following the proposed symmetrical conditions for the planar transformer in this paper, the planar transformer can be ensured to have a symmetrical winding structure and minimized CM noise when applied in a FB *LLC* converter before it is physically fabricated. The experimental results of a 360 W *LLC* converter show that the CM noise can be reduced significantly by around 11 dBμV (a reduction of around 4 times) at the fundamental frequency in both boost and buck mode operation ranges of the FB *LLC* prototype. This reduction in CM noise allows for a reduction in the size of the CM EMI filter, which helps to improve the power density of the whole system. It is noted that no additional cost is needed to achieve the CM noise reduction.



(a)



(b)

Fig. 12. Measured CM noise spectra. (a) Boost mode ($f_s < f_r$), V_{in} = 180V, f_s = 135 kHz. (b) Buck mode ($f_s > f_r$), V_{in} = 210V, f_s = 165 kHz.

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